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FDG315N

N-Channel Logic Level PowerTrench® MOSFET

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

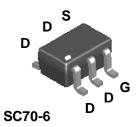
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

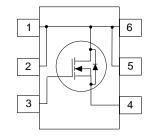
Applications

- DC/DC converter
- Load switch
- Power Management

Features

- 2 A, 30 V. $R_{DS(ON)} = 0.12~\Omega$ @ $V_{GS} = 10~V$ $R_{DS(ON)} = 0.16~\Omega$ @ $V_{GS} = 4.5~V$.
- Low gate charge (2.1nC typical).
- High performance trench technology for extremely low R_{ns/own}.
- Compact industry standard SC70-6 surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|-------------------|--|-----------|-------------|-------|
| V_{DSS} | Drain-Source Voltage | | 30 | V |
| V_{GSS} | Gate-Source Voltage | | ±20 | V |
| I _D | Drain Current - Continuous | (Note 1a) | 2 | Α |
| | - Pulsed | | 6 | |
| P _D | Power Dissipation for Single Operation | (Note 1a) | 0.75 | W |
| | | (Note 1b) | 0.48 | |
| T_J , T_{stg} | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

Thermal Characteristics

| $R_{\theta,IA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 260 | °C/W |
|-----------------|---|-----------|-----|------|
|-----------------|---|-----------|-----|------|

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|---------|-----------|------------|------------|
| .15 | FDG315N | 7" | 8mm | 3000 units |

| Symbol | Parameter | Test Conditions | Min | Тур | Max | Units |
|---------------------------------------|---|--|-----|-------------------------|----------------------|-------|
| Off Char | acteristics | | | • | I. | • |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$ | 30 | | | V |
| ΔBV _{DSS} ΔT _J | Breakdown Voltage Temperature Coefficient | I_D = 250 μ A, Referenced to 25°C | | 26 | | mV/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 24 V, V _{GS} = 0 V | | | 1 | μΑ |
| I _{GSS} | Gate-Body Leakage Forward | V _{GS} = 16 V, V _{DS} = 0 V | | | 100 | nA |
| I _{GSS} | Gate-Body Leakage Reverse | $V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$ | | | -100 | nA |
| On Char | acteristics (Note 2) | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | 1 | 1.8 | 3 | V |
| $\Delta V_{GS(th)} \over \Delta T_J$ | Gate Threshold Voltage Temperature Coefficient | I_D = 250 μ A, Referenced to 25°C | | -4 | | mV/°C |
| R _{DS(on)} | Static Drain-Source On-Resistance | $V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 4.5 \text{ V}, I_D = 1.7 \text{ A}$ | | 0.100 0.140 0.130 | 0.12 0.20 0.16 | Ω |
| I _{D(on)} | On-State Drain Current | $V_{GS} = 4.5 \text{ V}, I_D = 1.7 \text{ A}$ $V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$ | 3 | | | Α |
| G _{FS} | Forward Transconductance | $V_{DS} = 5 \text{ V}, I_{D} = 2 \text{ A}$ | | 5 | | S |
| Dynamic | Characteristics | | | | | |
| Ciss | Input Capacitance | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ | | 220 | | pF |
| Coss | Output Capacitance | f = 1.0 MHz | | 50 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 20 | | pF |
| Switchin | g Characteristics (Note 2) | | | | | |
| I _{d(on)} | Turn-On Delay Time | $V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$ | | 3 | 6 | ns |
| t _r | Turn-On Rise Time | $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$ | | 11 | 22 | ns |
| t _{d(off)} | Turn-Off Delay Time | | | 7 | 14 | ns |
| t _f | Turn-Off Fall Time | 1 | | 3 | 6 | ns |
| Qg | Total Gate Charge | $V_{DS} = 15 \text{ V}, I_D = 2 \text{ A},$ | | 2.1 | 4 | nC |
| Q _{gs} | Gate-Source Charge | $V_{GS} = 5 \text{ V}$ | | 0.8 | | nC |
| Q _{gd} | Gate-Drain Charge | 1 | | 0.7 | | nC |
| Drain-Sc | ource Diode Characteristics | and Maximum Ratings | | | | |
| I _S | Maximum Continuous Drain-Source | | | | 0.42 | А |
| V _{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_{S} = 0.42 \text{ A}$ (Note 2) | | 0.7 | 1.2 | V |

Notes

- a) 170°C/W when mounted on a 1 in $^2 pad$ of 20z copper.
- b) 260°C/W when mounted on a minimum pad.
- 2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

^{1.} R_{BUA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BUC} is guaranteed by design while R_{BCA} is determined by the user's board design.

Typical Characteristics

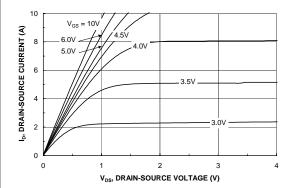


Figure 1. On-Region Characteristics.

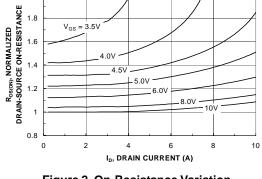


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

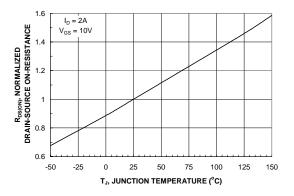


Figure 3. On-Resistance Variation with Temperature.

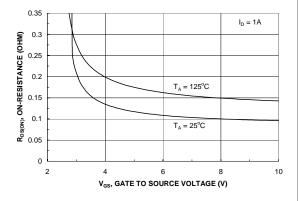


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

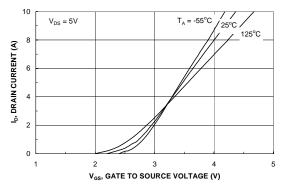


Figure 5. Transfer Characteristics.

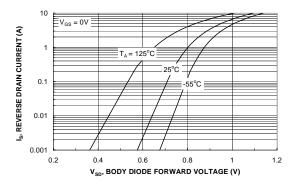


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

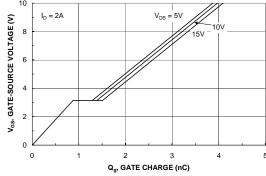


Figure 7. Gate-Charge Characteristics.

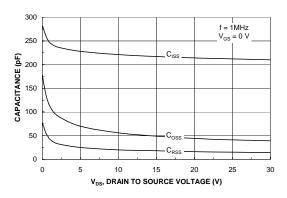


Figure 8. Capacitance Characteristics.

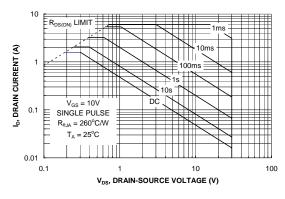


Figure 9. Maximum Safe Operating Area.

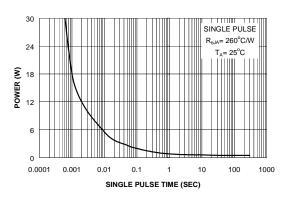


Figure 10. Single Pulse Maximum Power Dissipation.

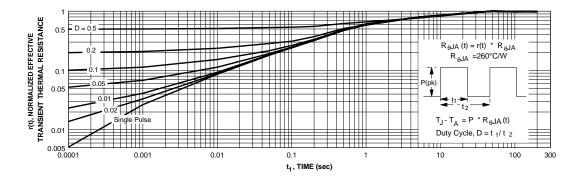


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.

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