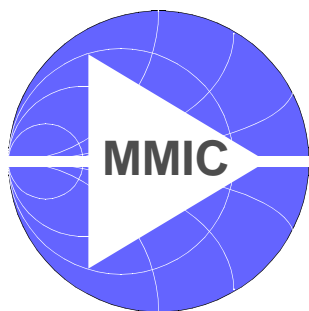


# BGB540

## Active Biased RF Transistor



Wireless  
Silicon Discretes



Never stop thinking.

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**BGB540****Data sheet****Revision History:        2002-09-11**

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Previous Version:        2001-08-16

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Page	Subjects (major changes since last revision)
4-9	RF parameters and SPICE model updated
	Preliminary status removed

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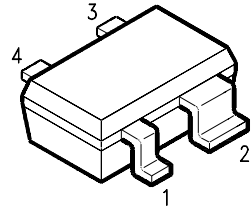
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## Active Biased RF Transistor

**BGB540**

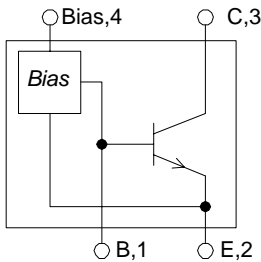
### Features

- $G_{ms} = 18\text{dB}$  at 1.8GHz
- Small SOT343 package
- Current easy adjustable by an external resistor
- Open collector output
- Typical supply voltage: 1.4-4.3V
- SIEGET<sup>®</sup>-45 technology



### Applications

- For high gain low noise amplifiers
- Ideal for wideband applications, cellular phones, cordless telephones, SAT-TV and high frequency oscillators



### Description

SIEGET<sup>®</sup>-45 NPN Transistor with integrated biasing for high gain low noise figure applications.  $I_C$  can be controlled using  $I_{Bias}$  according to  $I_C = 10 * I_{Bias}$ .

**ESD:** Electrostatic discharge sensitive device, observe handling precaution!

Type	Package	Marking	Chip
BGB540	SOT343	MCs	T0559

## Maximum Ratings

Parameter	Symbol	Value	Unit
Maximum collector-emitter voltage	$V_{CE}$	4.5	V
Maximum collector current	$I_C$	80	mA
Maximum bias current	$I_{Bias}$	8	mA
Maximum emitter-base voltage	$V_{EB}$	1.2	V
Maximum base current	$I_B$	0.7	mA
Total power dissipation, $T_S < 75^\circ\text{C}^{1)}$	$P_{tot}$	250	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Ambient temperature	$T_A$	-65 ... +150	$^\circ\text{C}$
Storage temperature	$T_{STG}$	-65 ... +150	$^\circ\text{C}$
Thermal resistance: junction-soldering point	$R_{th\ JS}$	300	K/W

Notes:

For detailed symbol description refer to figure 1.

<sup>1)</sup>  $T_S$  is measured on the emitter lead at the soldering point to the PCB

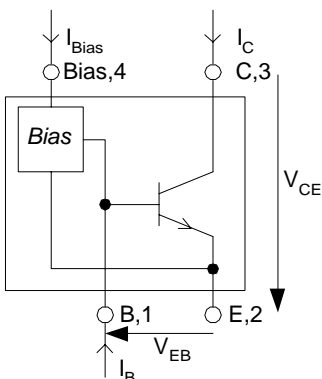


Fig. 1: Symbol definition

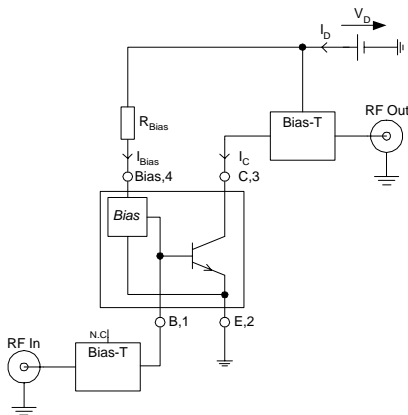


Fig. 2: Test Circuit for Electrical Characteristics and S-Parameter

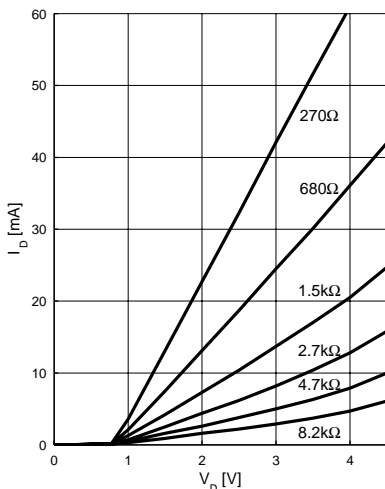
**Electrical Characteristics** at  $T_A=25^\circ\text{C}$  (measured in test circuit specified in fig. 2)

Parameter	Symbol	min.	typ.	max.	Unit
Maximum stable power gain $V_D=2\text{V}$ , $I_c=20\text{mA}$ , $f=1.8\text{GHz}$	$G_{ms}$		18		dB
Insertion power gain $V_D=2\text{V}$ , $I_c=20\text{mA}$	$ S_{21} ^2$	$f=0.9\text{GHz}$ $f=1.8\text{GHz}$	21.5 16		dB
Insertion loss $V_D=2\text{V}$ , $I_c=0\text{mA}$	IL	$f=0.9\text{GHz}$ $f=1.8\text{GHz}$	21 16		dB
Noise figure ( $Z_S=50\Omega$ ) $V_D=2\text{V}$ , $I_c=5\text{mA}$	$F_{50\Omega}$	$f=0.9\text{GHz}$ $f=1.8\text{GHz}$	1.15 1.3		dB
Output power at 1dB gain compression $V_D=2\text{V}$ , $I_c=20\text{mA}$ , $f=1.8\text{GHz}$	$P_{-1\text{dB}}$	$Z_L=Z_{LOPT}$ $Z_L=50\Omega$	12 10		dBm
Output third order intercept point $V_D=2\text{V}$ , $I_c=20\text{mA}$ , $f=1.8\text{GHz}$	$OIP_3$	$Z_{L/S}=Z_{L/SOPT}$ $Z_{L/S}=50\Omega$	22 20		dBm
Collector-base capacitance $V_{CB}=2\text{V}$ , $f=1\text{MHz}$	$C_{CB}$		0.15		pF
Current ratio $I_c/I_{Bias}$ $I_{Bias}=0.5\text{mA}$ , $V_D=3\text{V}$	CR		7	13	

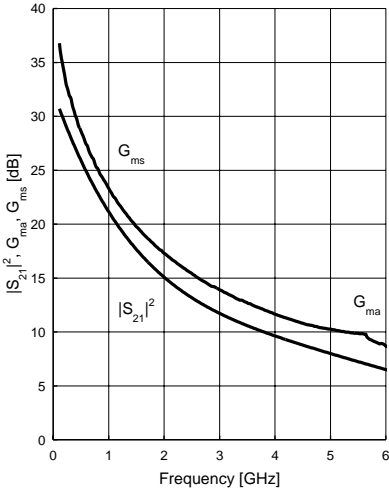
**S-Parameter**  $V_D=2V$ ,  $I_C=20mA$  (see Electrical Characteristics for conditions)

Frequency [GHz]	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	0.5387	-17.8	35.6280	158.9	0.0064	75.4	0.9334	-11.8
0.2	0.4744	-35.8	31.0390	142.8	0.0141	76.8	0.8357	-20.9
0.4	0.3724	-60.7	22.5520	120.2	0.0241	75.4	0.6670	-29.7
0.6	0.2992	-74.7	16.8920	108.1	0.0335	75.3	0.5672	-31.0
0.8	0.2453	-88.7	13.3320	98.2	0.0439	74.7	0.5066	-33.0
1.0	0.2205	-100.1	10.9000	91.2	0.0547	73.4	0.4675	-33.8
1.2	0.1900	-111.0	9.1938	85.5	0.0663	71.5	0.4406	-35.1
1.4	0.1765	-122.0	7.9452	80.6	0.0785	69.3	0.4209	-36.8
1.6	0.1648	-132.7	6.9615	76.3	0.0901	66.5	0.4013	-38.7
1.8	0.1660	-142.5	6.2388	72.2	0.1014	63.5	0.3822	-41.5
2.0	0.1737	-153.1	5.6320	68.2	0.1125	60.5	0.3519	-43.6
3.0	0.1966	175.9	3.8040	51.6	0.1655	44.9	0.2868	-57.0
4.0	0.2486	156.8	2.9394	36.2	0.2151	29.1	0.2398	-76.1
5.0	0.3451	136.5	2.4109	20.7	0.2439	9.1	0.1506	-111.0
6.0	0.4645	117.1	2.0318	5.5	0.2362	-7.1	0.1196	168.0

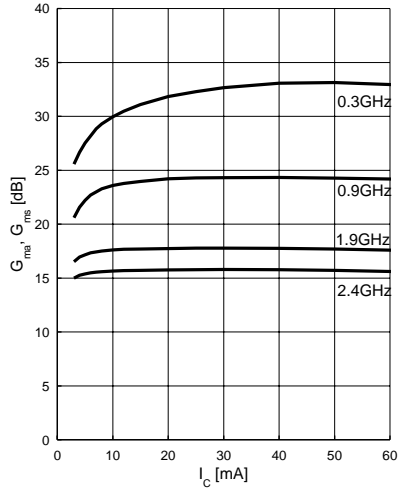
**Device Current**  $I_D = f(V_D, R_{Bias})$



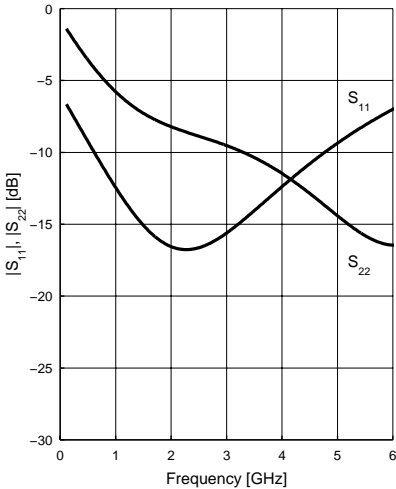
**Power Gain**  $|S_{21}|^2, G_{ma}, G_{ms} = f(f)$   
 $V_D = 3V, I_C = 20mA$



**Power Gain**  $G_{ma}, G_{ms} = f(f)$   
 $V_D = 3V$

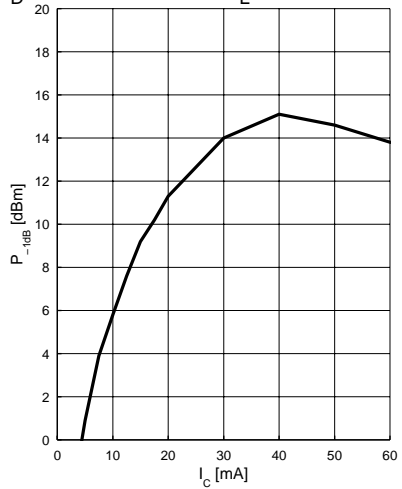


**Matching**  $|S_{11}|, |S_{22}| = f(f)$   
 $V_D = 3V, I_C = 20mA$



**Output Compression Point**

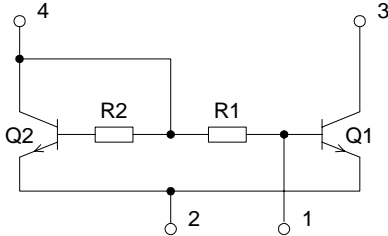
$P_{-1dB} = f(I_C)$   
 $V_D = 3V, f = 1.8GHz, Z_L = 50\Omega$





## SPICE Model

### BGB540-Chip



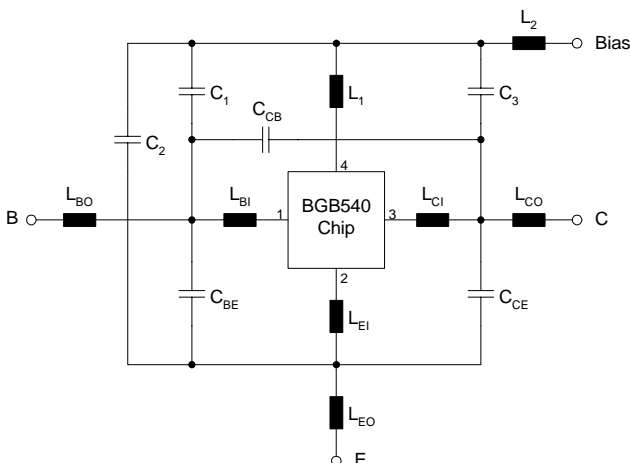
Q1	T513
Q2	T513 (area factor: 0.1)
R1	2.7kΩ
R2	27kΩ

### Transistor Chip Data T513 (Berkley-SPICE 2G.6 Syntax)

.MODEL T513 NPN(

+ IS = 8.2840e-17	BF = 107.5	NF = 1.0	VAF = 28.383
+ IKF = 0.48731	ISE = 1.115e-11	NE = 3.19	BR = 5.5
+ NR = 1.0	VAR = 19.705	IKR = 0.02	ISC = 1.9237e-17
+ NC = 1.1720	RBM = 1.3	IRB = 0.00072983	RB = 5.4
+ RE = 0.31111	RC = 4.0	CJE = 1.8063e-15	VJE = 0.8051
+ MJE = 0.46576	TF = 6.76e-12	XTF = 0.4219	VTF = 0.23794
+ ITF = 0.001	PTF = 0	CJC = 2.34e-13	VJC = 0.81969
+ MJC = 0.30232	XCJC = 0.3	TR = 2.324E-09	CJS = 0
+ VJS = 0.75	MJS = 0	XTB = 0	EG = 1.11
+ XTI = 3	FC = 0.73234)		

### Package Equivalent Circuit



L <sub>BI</sub>	0.36 nH
L <sub>BO</sub>	0.42 nH
L <sub>EI</sub>	0.35 nH
L <sub>EO</sub>	0.27 nH
L <sub>CI</sub>	0.56 nH
L <sub>CO</sub>	0.58 nH
L <sub>1</sub>	0.5 nH
L <sub>2</sub>	0.58 nH
C <sub>BE</sub>	120 fF
C <sub>CB</sub>	6.9 fF
C <sub>CE</sub>	134 fF
C <sub>1</sub>	90 fF
C <sub>2</sub>	120 fF
C <sub>3</sub>	15 fF

Valid up to 3GHz

### Typical Application

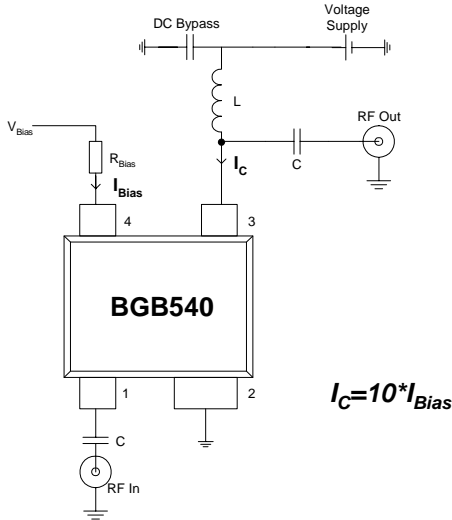
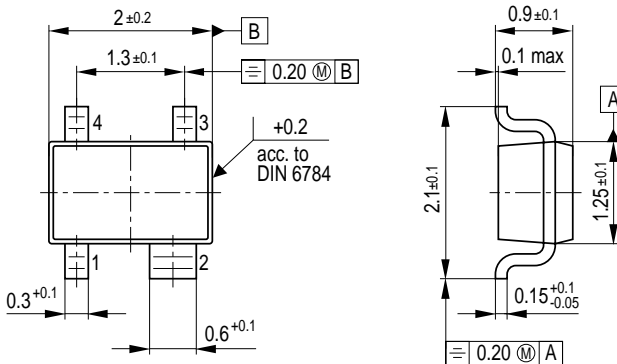


Fig. 3: Typical application circuit

This proposal demonstrates how to use the BGB540 as a Self-Biased Transistor. As for a discrete Transistor matching circuits have to be applied. A good starting point for various applications are the Application Notes provided for the BFP540.

### Package Outline



GPS05605