QUAD POWER FAULT MONITOR

Description

The SG1548 is an integrated circuit capable of monitoring up to four positive DC supply voltages simultaneously for overvoltage and undervoltage fault conditions. An on-chip inverting op amp also allows monitoring one negative DC voltage. The fault tolerance window is accurately programmable from ±5% to ±40% using a simple divider network on the 2.5V reference. A single external capacitor sets the fault indication delay, eliminating false outputs due to switching noise, logic transition current spikes, and short-term AC line interruptions.

An additional comparator referenced to 2.5V allows the AC line to be monitored for undervoltage conditions or for generation of a line clock. The comparator can also be used for programmable undervoltage lockout in a switching power supply. Uncommitted collector and emitter outputs permit both inverting and non-inverting operation. External availability of the precision 2.5V reference and open-collector logic outputs permit expansion to monitor additional voltage using available open-collector quad comparators.

Features

- Monitors Four DC Voltages and the AC Line
- Precision 2.5V ±1% Low-drift Reference
- Fault Tolerance Adjustable from ±5% to ±40%
- ±3% Trip Threshold Tolerance over Temperature
- Separate 10mA, 40V Overvoltage, Undervoltage, and AC line Fault Outputs
- Fault Delay Programmable with a Single Capacitor
- 30mV Comparator Hysteresis to Prevent Oscillations
- On-Chip Inverting Op-Amp for Negative Voltage
- Open-Collector Output Logic or Expandability
- Operation from 4.5V to 40V Supply

High Reliability Features

Following are the high reliability features of SG1548:

- Available to MIL-STD-883, ¶ 1.2.1
- Radiation data available
- MSC-AMS level "S" processing available

Block Diagram

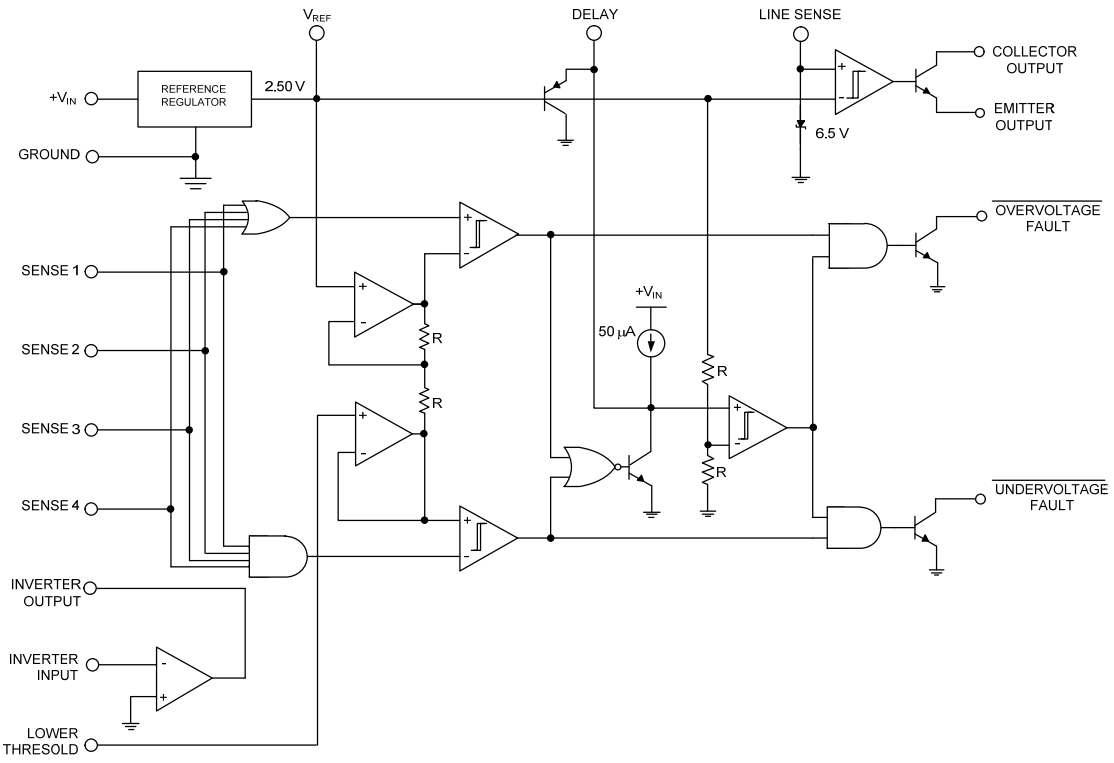
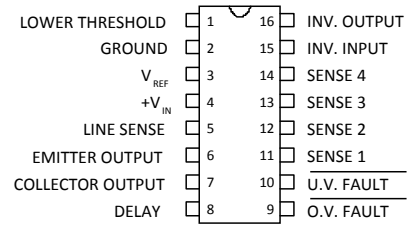
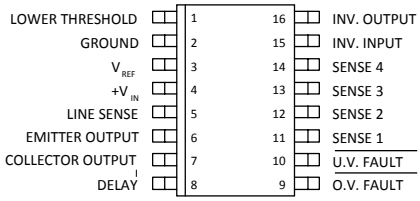
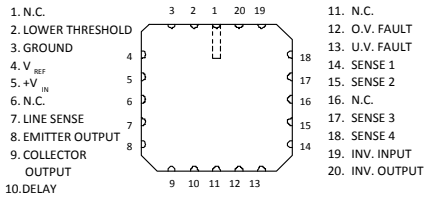


Figure 1 · Block Diagram

Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	J	16-PIN CERAMIC DIP	SG1548J-883B SG1548J	CERDIP	 N package: Pb-free / RoHS 100% Matte Tin Lead Finish
-25°C to 85°C 0°C to 70°C	N	16-PIN PLASTIC DIP	SG2548N* SG3548N*	PDIP	
-25°C to 85°C 0°C to 70°C	DW	16-PIN SMALL-OUTLINE WIDE BODY	SG2548DW* SG3548DW*	SOWB	 DW package: Pb-free / RoHS 100% Matte Tin Lead Finish
-55°C to 125°C	L	20-PIN CERAMIC (LCC)	SG1548L-883B SG1548L	CLCC	

Notes:

1. *Contact factory for DESC product availability.*
2. *All parts are viewed from the top.*
3. *Hermetic Packages J & L use Pb37/Sn63 hot solder lead finish, contact factory for availability of RoHS versions.*

**RoHS Compliant*

Absolute Maximum Ratings[1]

Parameter	Value	Units
Supply Voltage ($+V_{IN}$)	40	V
Fault Output Collector Voltage	40	V
Sense Input Voltage Range	-0.3V to 6.0V	V
Fault Output Sink Current	20	mA
Line Sense Input Current	±1	mA
Inverting Op Amp Input Current	-5	mA
Inverting Op Amp Output Current	25	mA
Operating Junction Temperature		
Hermetic (J, L Packages)	150	°C
Plastic (N, DW Packages)	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature	300	°C

Notes:
1. *Values beyond which damage may occur.*
2. *Pb-free / RoHS Peak Package Solder Reflow Temp. (40 second max. exposure). 260°C (+0, -5)*

Thermal Data

Parameter	Value	Units
J Package		
Thermal Resistance-Junction to Case, θ_{JC}	30	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	80	°C/W
N Package		
Thermal Resistance-Junction to Case, θ_{JC}	40	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	65	°C/W
DW Package		
Thermal Resistance-Junction to Case, θ_{JC}	40	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	95	°C/W
L Package		
Thermal Resistance-Junction to Case, θ_{JC}	35	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W

Notes:
1. *Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.*
2. *The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.*

Recommended Operating Conditions[1]

Supply Voltage Range	Value	Units
±25% Maximum Fault Window [2]	4.5 to 35	V
±40% Maximum Fault Window	5.0 to 35	V
Lower Threshold Input Range	1.5 to 2.45	V
Fault Tolerance Window Range	±5 to ±40	%
Fault Output Sink Current Range	0 to 10	mA
Line Sense Output Current Range	0 to 10	mA
Voltage Reference Output Current	0 to 10	mA
Operating Ambient Temperature Range		
SG1548	-55 to 125	°C
SG2548	-25 to 85	°C
SG3548	0 to 70	°C

Notes:
1. *Range over which the device is functional.*
2. *Limited by inverter amplifier positive swing at -55°C.*

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1548 with -55°C ≤ T_A ≤ 125°C, SG2548 with -25°C ≤ T_A ≤ 85°C, SG3548 with 0°C ≤ T_A ≤ 70°C, and $+V_{IN}$ = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Test Conditions	SG1548/2548			SG3548			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Section								
Supply Current	$+V_{IN}$ = 40V		4.8	10		4.8	10	mA
Reference Section(1)								
Output Voltage	T_J= 25°C	2.475	2.500	2.525	2.475	2.500	2.525	V
	Over Temperature	2.450		2.550	2.450		2.550	V
Line Regulation	$+V_{IN}$ = 4.5V to 35V		1	5		1	5	mV
Load Regulation	I_L = 0 to 10mA		3	10		3	10	mV
Short Circuit Current	V_{REF} = 0V	10	25	50	10	25	50	mA
Fault Window Generator Section								
Input Bias Current	$V_{PIN\ 1}$ = 1.5V to 2.45V		-0.4	-2.0		-0.4	-2.0	µA
DC Sense Inputs Section								
Overvoltage Threshold	$V_{PIN\ 1}$ = 0.95 x V_{REF}	2.547	2.625	2.704	2.547	2.625	2.704	V
	$V_{PIN\ 1}$ = 0.60 x V_{REF}	3.396	3.500	3.606	3.396	3.500	3.606	V
Undervoltage Threshold	$V_{PIN\ 1}$ = 0.95 x V_{REF}	2.304	2.375	2.447	2.304	2.375	2.447	V
	$V_{PIN\ 1}$ = 0.60 x V_{REF}	1.455	1.500	1.545	1.455	1.500	1.545	V
Input Bias Current	V_{SENSE} = 1.5V to 3.5V		±0.6	±2.0		±0.6	±2.0	µA
Threshold Supply Rejection	$+V_{IN}$ = 4.5V to 35V	60	100		60	100		dB
Fault Delay Section								
Comparator Threshold		1.200	1.250	1.300	1.200	1.250	1.300	V
Comparator Hysteresis			25			25		mV
Delay Charging Current	$V_{PIN\ 8}$ = 0V	32.5	50	67.5	32.5	50	67.5	µA
On Saturation Voltage	$I_{PIN\ 8}$ = 0mA		0.1	0.2		0.1	0.2	V
OFF Clamp Voltage	$I_{PIN\ 8}$ = 0mA		+3.2	+3.6		+3.2	+3.6	V
Inverting Op Amp Section(2)								
Input Offset Voltage			2	15		2	15	mV
Input Bias Current			-0.3	-1.0		-0.3	-1.0	µA
Output High Voltage	I_{SOURCE} = 5mA	3.2	3.5		3.2	3.5		V
Output Low Voltage	I_{SINK} = 5mA		1.0	1.9		1.0	1.9	V
Large Signal Voltage Gain	R_L = 10k	72	100		72	100		dB
Output Source Current		5	15	25	5	15	25	mA
Power Supply Rejection Ratio	$+V_{IN}$ = 4.5V to 35V	72	100		72	100		dB
AC Line Sense Section								
Comparator Threshold	$V_{PIN\ 5}$ = Low to High	2.440	2.500	2.560	2.440	2.500	2.560	V
Comparator Hysteresis			25			25		mV
Input Bias Current	$V_{PIN\ 5}$ = 2.5V		1	2		1	2	µA
Collector Leakage Current	V_{CE} = 40V		1	10		1	10	µA
Collector Saturation Voltage	I_C= 10mA		0.2	0.5		0.2	0.5	V
Emitter Output Voltage	I_E = 10mA	12	13		12	13		V
Diode Clamp Voltage	$I_{PIN\ 5}$ = 1mA	6.0		7.5	6.0		7.5	V
	$I_{PIN\ 5}$ = -1mA	-0.3		-1.0	-0.3		-1.0	V
Fault Logic Outputs (Each output)								
Collector Leakage Current	V_C = 40V		1	10		1	10	µA
Collector Saturation Voltage	I_C = 10mA		0.2	0.5		0.2	0.5	V

Notes:
1. I_L = 0mA
2. $+V_{IN}$ = 4.5V.

Application Information

Setting the Fault Tolerance Window

The fault tolerance window is set by applying a voltage less than the +2.50Vreference to the Lower Threshold input (Pin 1). The voltage is obtained by a resistor divider from the reference (Pin 3) to ground. If ±5% tolerance is desired, then 95% of the reference (+2.375V) is applied to Pin 1. If ±40% is wanted, then 60% of the reference (+1.50V) is applied. In the example on the back page, the tolerance is ±5%. The nominal overvoltage and undervoltage thresholds are centered about the reference at +2.625V and +2.375V (+2.500V ±0.125V).

Scaling the Monitored Supply Voltages

Each positive voltage to be monitored is divided down to +2.50V with a resistor network and connected to one of the Sense inputs. Unused Sense inputs should be connected to the reference. This will not increase the bias current. A variation of the monitored voltages out of the programmed tolerance range will cause the appropriate overvoltage or undervoltage fault output to switch LOW. The effective tolerance on any input may be broadened with an additional resistor to the voltage reference. The example on the back page shows a ±10% tolerance on the +5Vsupply although the SG1548 is programmed for a ±5% tolerance. The procedure for calculating the resistor value is found in the SG1548 Application Note.

Monitoring a Negative Voltage

A negative voltage can be converted to a positive one and simultaneously scaled to +2.50V by using the internal operational amplifier as an inverter. Only an input resistor and feedback resistor are required.

Setting the Fault Delay

A single capacitor at the Delay pin sets the time an out-of tolerance fault must persist before a fault is actually declared. This feature allows switching noise on the supplies to be rejected. The delay time is given by: Delay = 25ms/μF.

AC Line Monitoring

The AC line voltage can be monitored for single-cycle dropouts with the few components shown in the example. A half-wave rectifier charges the capacitor on positive line cycles. After the positive peak and during the negative line cycle the capacitor discharges from a fixed voltage controlled by the internal Zener diode. If a positive cycle is missing, the capacitor discharges to below the +2.5V trip point of the comparator, causing the output transistor to turn on.

Application Example

In this example, the SG1548 simultaneously monitors four DC voltages: +5V, +24V, and ±15V. Three different fault tolerances are programmed: ±5% on the two 15V supplies, ±10% on the +5V supply, and ±20% on the +24V supply. The 5µF delay capacitor provides 125 milliseconds of fault delay.

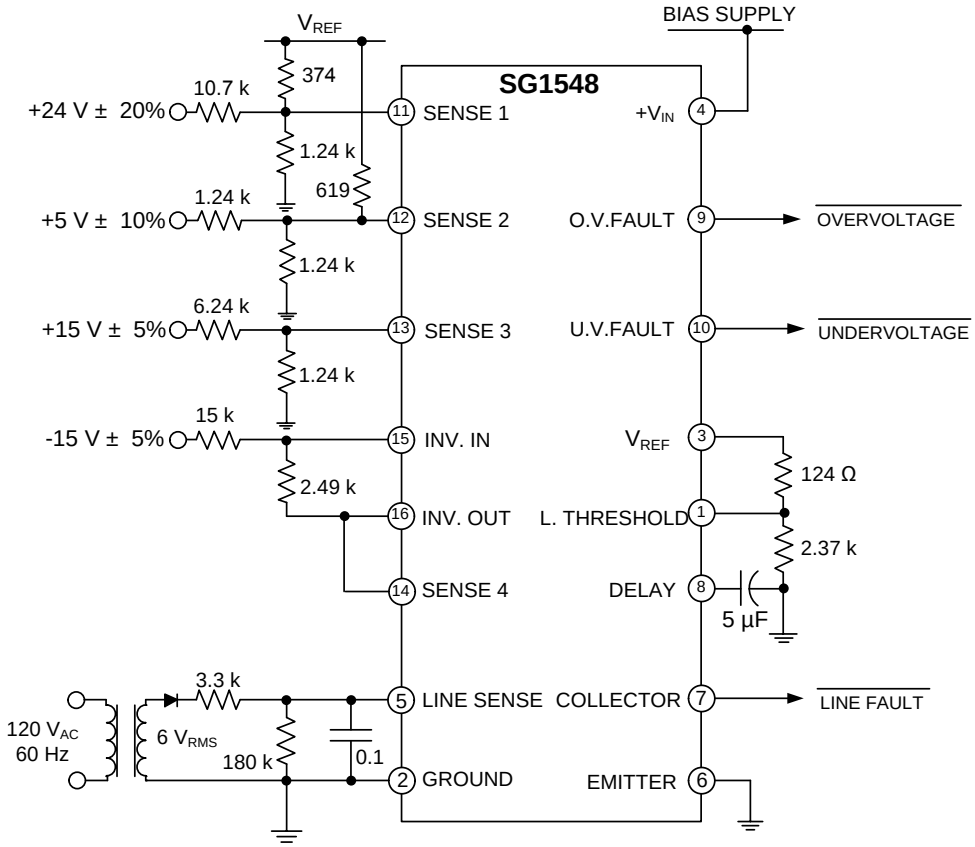
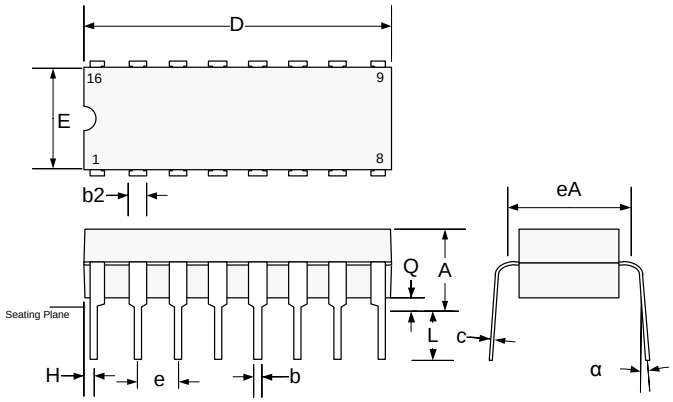


Figure 2 · Application Example

Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.



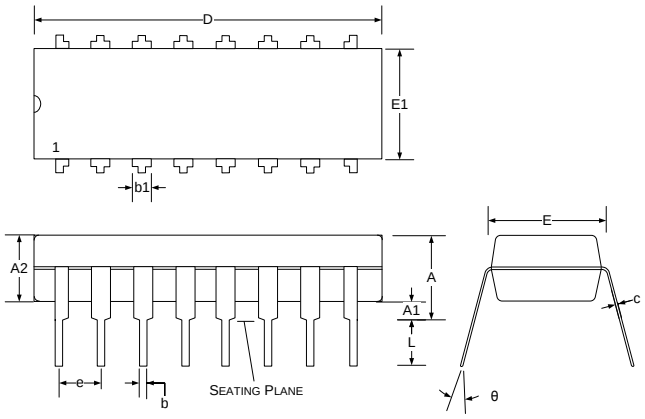
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		5.08		0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

*

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 3 · J 16-Pin Ceramic Dip



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		5.33		0.210
A1	0.38		0.015	
A2	3.30 Typ.		0.130 Typ.	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	0.381	0.115	0.150
θ	-	15°	-	15°

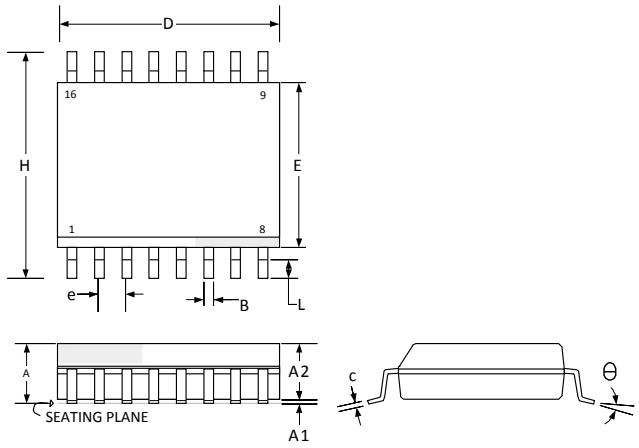
Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 11 · N 16-Pin Plastic Dip

Package Outline Dimensions (continued)

Controlling dimensions are in inches, metric equivalents are shown for general information.

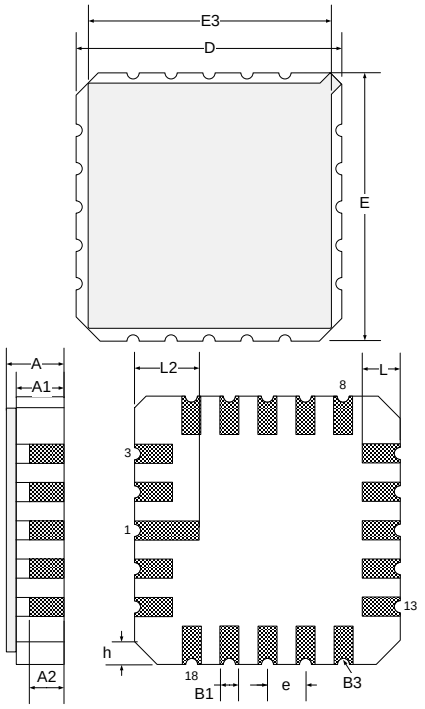


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.06	2.65	0.081	0.104
A1	0.10	0.30	0.004	0.012
A2	2.03	2.55	0.080	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	10.08	10.50	0.397	0.413
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
Θ	0°	8°	0°	8°
*LC	–	0.10	–	0.004

Note:

1. Controlled dimensions are in mm, inches are for reference only.
2. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 12 · DW 16-Pin Plastic Wide-body SOIC



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 13 · 20-Pin Ceramic Leadless Chip Carrier

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