Kinetis MCU ARM® Powered Portfolio Overview

AMF-CON-T0483

Ronald Lowman

August 2013

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Agenda

- Kinetis Portfolio - Baseline
- Kinetis K – CSP Packaging
- Kinetis K – Security Expansion
- Kinetis K - Memory Expansion
- Kinetis K – FPU Expansion
- Kinetis L - Low Power
- Kinetis E - 5V Robust
- Kinetis V – Motor Control
- Kinetis M - Metering
- Kinetis W – Wireless

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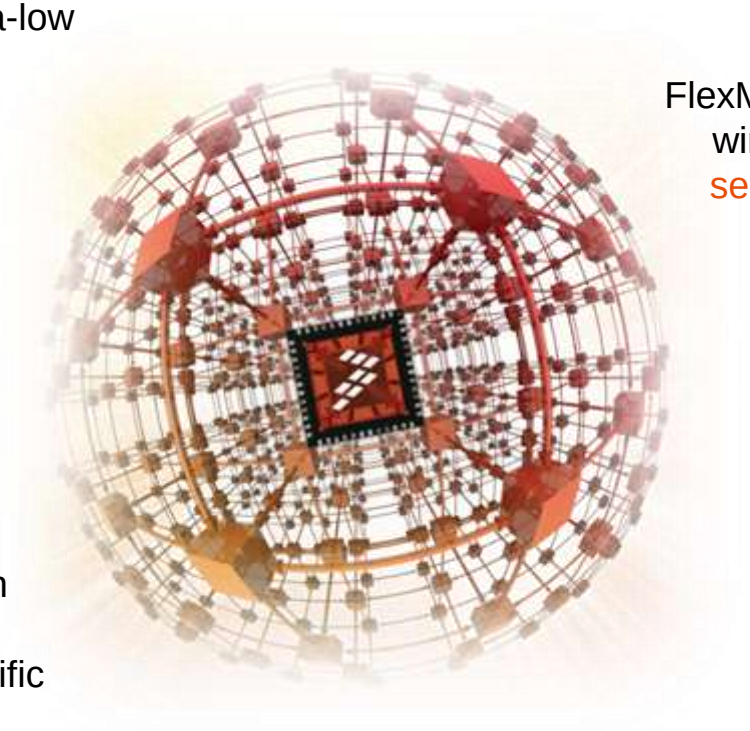
Kinetis: Freescale ARM® Cortex-M MCUs

Design Potential. Realized

ARM® Cortex™-M

Over 300 **compatible** ultra-low power ARM Cortex-M0+ and high-performance ARM Cortex-M4 MCUs with scalable performance, memory and feature integration



Integration

Huge peripheral choice with high-precision mixed-signal, FlexMemory (EEPROM), wired & wireless connectivity, HMI and security features for consumer and industrial applications

Scalability

- Entry-level to feature-rich
- 8 KB-1 MB, 16 pin to 256 pin
- Low power & 5 V/high EMC
- Standard & application-specific

Enablement

Freescale Tower System, bundled MQX RTOS and CodeWarrior IDE with Processor Expert auto code generator. Broad third-party support from IAR, KEIL, Green Hills and others

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Kinetis ARM Cortex MCU Portfolio (General Purpose)

Performance

ARM Cortex-M4 powered

Kinetis K Series
Industry-first **ARM Cortex-M4** MCU families from 50MHz / 32KB with low power, FlexMemory, mixed-signal and broad connectivity, HMI & security features.

Alpha Samples: Q4 2010
Production: Now

Kinetis L Series
Ultra-low power/cost **ARM Cortex-M0+** MCU families from 32MHz / 8KB with mixed-signal, connectivity & HMI features in low pin-count packages. Compatible with 'K' Series & S08Px
Alpha Samples: Q3 2012
Production: Q4 2012

Kinetis E Series
Robust, low cost **5V ARM Cortex-M0+** MCU families for use in high electrical noise environments. Safety features for high-reliability applications. Compatible with S08Px and 'L' Series
Alpha Samples: Apr 2013
Production: July 2013

ARM Cortex-M0+ powered

Integration

Leading Performance - Low Power - Scalability - Industrial-grade reliability & temp

Freescale Bundled IDE, RTOS & Middleware - Rapid prototyping Platform - Broad ARM Ecosystem Support

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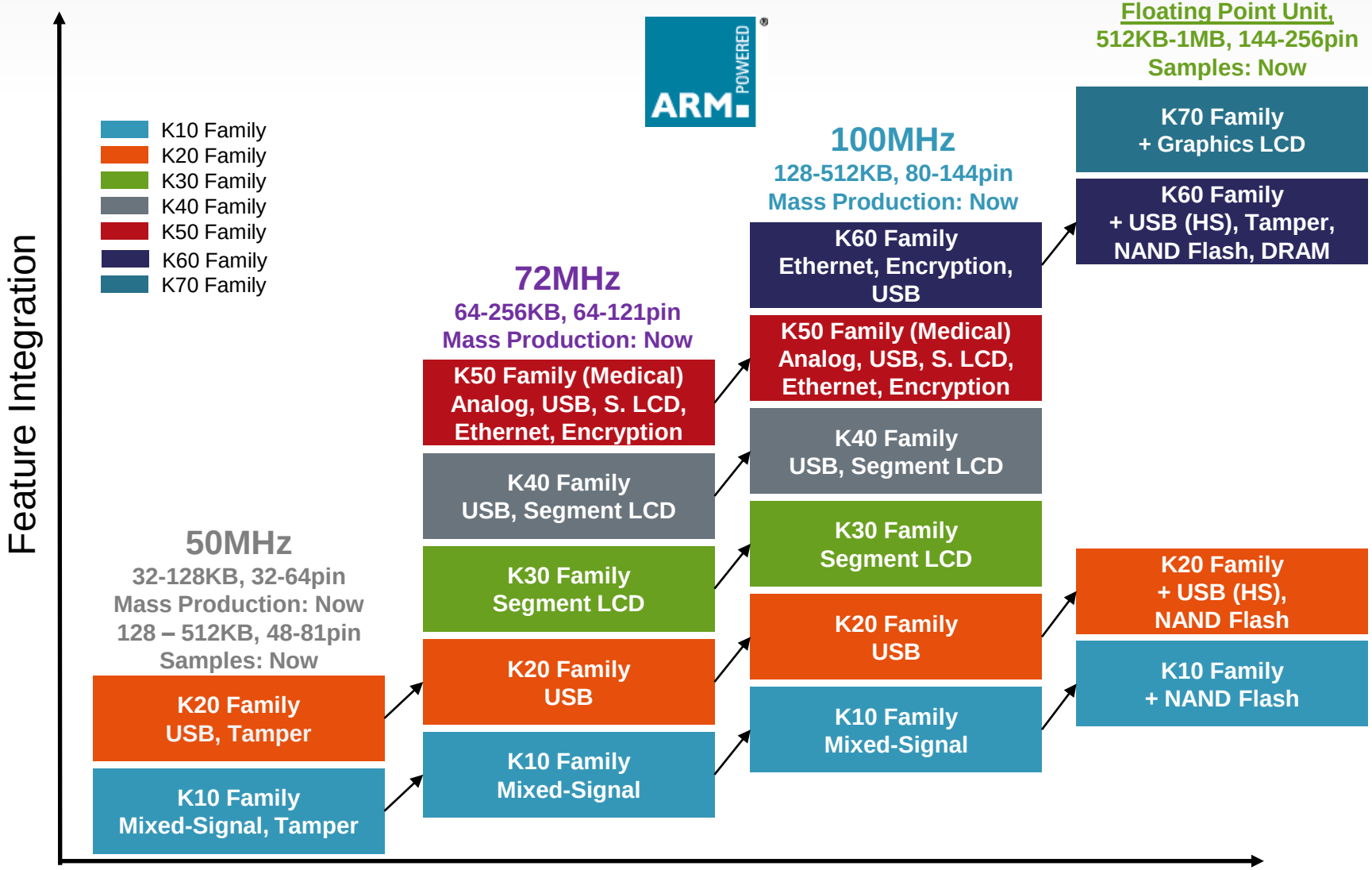
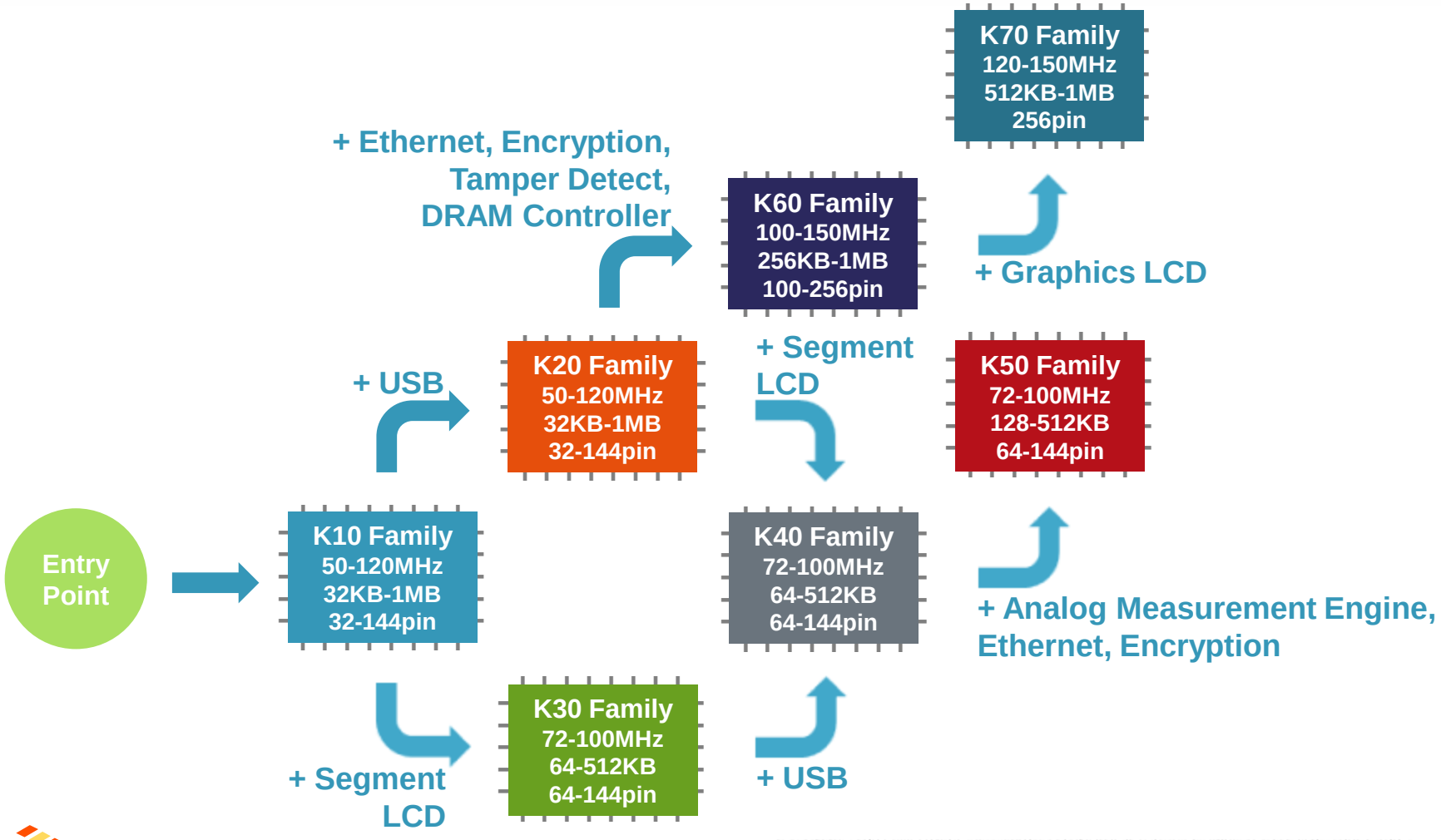
...netis K Series: Scalable MCUs based on the ARM Cortex-M4 core



netis K Series: MCU Family Compatibility

Hardware & software compatible MCU families with scalable performance, memory and feature integration



Kinetis K20 Family

Core
- Arm® Cortex™- M4 50/72/100/120 MHz
- Debug Interfaces
- DSP
- Interrupt Controller
- Float Point Unit (FPU)

System
- Internal and External Watchdogs
- Memory Protection Unit (MPU)
- DMA
- Low–Leakage Wake-Up Unit

Memories
- Program Flash (32 KB to 1 MB)
- SRAM (8 to 128 KB)
- FlexMemory (32 to 512 KB) (2 to 16 KB EE)
- External Bus Interface (FlexBus)
- Serial Programming Interface (EZPort)
- Cache
- NAND Flash Controller

Clocks
- Phase-Locked Loop
- Flequency-Locked Loop
- Low/High-Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Random Number Generator
- Cryptographic Acceleration Unit
- Hardware Tamper Detection Unit

Analog
- 16-bit ADC
- PGA
- Analog Comparator with 6-bit DAC
- 12-bit DAC
- Voltage Reference

Timers
- FlexTimer
- Carrier Modulator Transmitter
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)

Communication Interfaces
- I^2C
- I^2S
- UART (ISO 7816)
- Secure Digital Host Controller (SDHC)
- SPI
- USB On-the-Go (LS/FS)
- CAN
- USB On-the-Go (HS)
- USB Device Charger Detect (DCD)
- USB Voltage Regulator

HMI
- GPIO
- Xtrinsic Low-Power Touch – Sensing Interface

Standard Feature Optional Feature

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Kinetis K60 Family

Core
- Arm® Cortex™- M4 100/120/150 MHz
- Debug Interfaces
- DSP
- Interrupt Controller
- Float Point Unit (FPU)

System
- Internal and External Watchdogs
- Memory Protection Unit (MPU)
- DMA
- Low–Leakage Wake-Up Unit

Memories
- Program Flash (256 to 1 MB)
- SRAM (64 to 128 KB)
- FlexMemory (256 to 512KB) (4 to 16 KB EE)
- External Bus Interface (FlexBus)
- Serial Programming Interface (EZPort)
- Cache
- NAND Flash Controller
- DDR Controller

Clocks
- Phase-Locked Loop
- Flequency-Locked Loop
- Low/High-Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Random Number Generator
- Cryptographic Acceleration Unit (CAU)
- Hardware Tamper Detection Unit

Analog
- 16-bit ADC
- PGA
- Analog Comparator with 6-bit DAC
- 12-bit DAC
- Voltage Reference

Timers
- FlexTimer
- Carrier Modulator Transmitter
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)
- IEEE® 1588 Timer

Communication Interfaces
- I²C
- I²S
- UART (ISO 7816)
- Secure Digital Host Controller (SDHC)
- SPI
- USB On-the-Go (LS/FS)
- CAN
- USB On-the-Go (HS)
- IEEE 1588 Ethernet MAC
- USB Device Charger Detect (DCD)
- USB Voltage Regulator

HMI
- GPIO
- Xtrinsic Low-Power Touch – Sensing Interface

☐ Standard Feature ⬚ Optional Feature

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Kinetis K70 Family

Core
- Arm® Cortex™- M4 120/150 MHz
- Debug Interfaces
- DSP
- Interrupt Controller
- Float Point Unit (FPU)

System
- Internal and External Watchdogs
- Memory Protection Unit (MPU)
- DMA
- Low–Leakage Wake-Up Unit

Memories
- Program Flash (512KB to 1 MB)
- FlexMemory (512KB) (16 KB EE)
- Serial Programming Interface (EZPort)
- NAND Flash Controller
- SRAM (128 KB)
- External Bus Interface (FlexBus)
- Cache
- DDR Controller

Clocks
- Phase-Locked Loop
- Flequency-Locked Loop
- Low/High-Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Random Number Generator
- Cryptographic Acceleration Unit (CAU)
- Hardware Tamper Detection Unit

Analog
- 16-bit ADC
- PGA
- Analog Comparator with 6-bit DAC
- 12-bit DAC
- Voltage Reference

Timers
- FlexTimer
- Carrier Modulator Transmitter
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)
- IEEE® 1588 Timer

Communication Interfaces
- I^2C
- UART (ISO 7816)
- SPI
- CAN
- IEEE 1588 Ethernet MAC
- I^2S
- Secure Digital Host Controller (SDHC)
- USB On-the-Go (LS/FS/HS)
- USB Device Charger Detect (DCD)
- USB Voltage Regulator

HMI
- GPIO
- Xtrinsic Low-Power Touch – Sensing Interface
- Graphic LCD Controller

Standard Feature Optional Feature

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Kinetis K Series Package Options

64MAPBGA
5 x 5 mm
0.5mm pitch
(K10/20)

121MAPBGA
8 x 8 mm
0.65mm pitch
(K10/20/30/40/50/60)

144MAPBGA
13 x 13 mm
1.0mm pitch
(K10/20/30/40/50/60)

256MAPBGA
17 x 17 mm
1.0mm pitch
(K60/70)

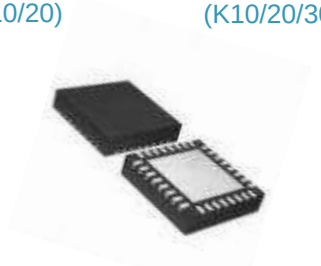
48LQFP
7 x 7 mm
0.55mm pitch
(K10/20)

64LQFP
10 x 10 mm
0.5mm pitch
(K10/20/30/40/50)

80LQFP
12 x 12 mm
0.5mm pitch
(K10/20/30/40/50)

100LQFP
14 x 14 mm
0.5mm pitch
(K10/20/30/40/50/60)

144LQFP
20 x 20 mm
0.5mm pitch
(K10/20/30/40/50/60)



32QFN
5 x 5 mm
0.5mm pitch
(K10/20)

48QFN
7 x 7 mm
0.5mm pitch
(K10/20)

121CSP
5 x 5 mm
0.4mm pitch
(K10/20/60)

143CSP
6 x 6 mm
0.4mm pitch
(K61)

Try the new online *Packaging Selector*

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DSP Family Summary
Kinetis K60 / K20 100MHz

Part Number	CPU (MHz)	Flash (KB)	SRAM (KB)	Temp Range	Other Features
MK20DN512ZAB10R	100	512	128	(0 ~ 70°C)	USB OTG (FS/HS)
MK60DN512ZAB10R	100	512	128	(0 ~ 70°C)	USB OTG (FS/HS), IEEE® 1588 Ethernet, Encryption
MK20DN512ZCAB10R	100	512	128	(-40 ~ 85°C)	USB OTG (FS/HS)
MK60DN512ZCAB10R	100	512	128	(-40 ~ 85°C)	USB OTG (FS/HS), IEEE® 1588 Ethernet, Encryption

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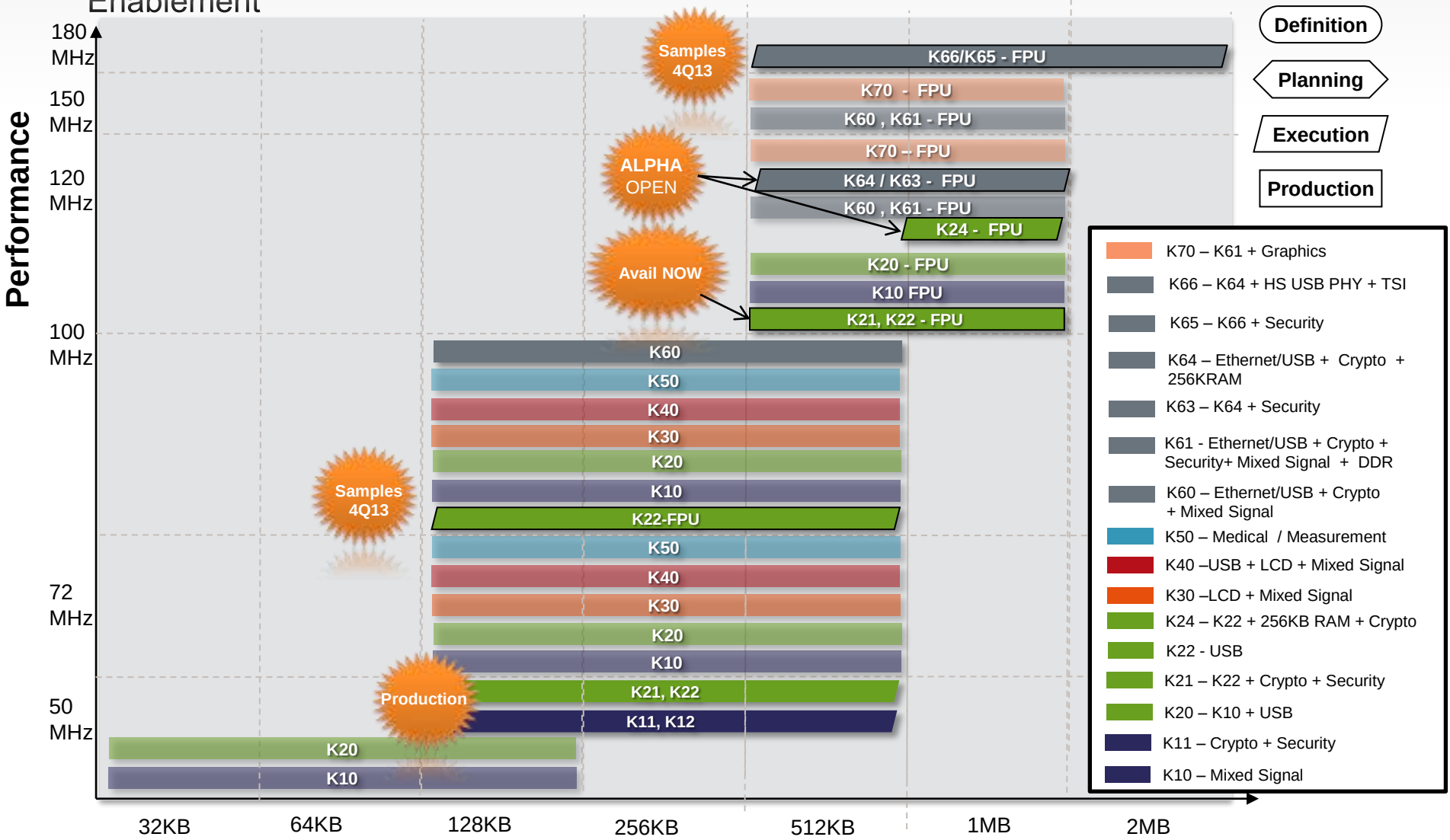
013 Kinetis K Series Roadmap

Scalable, Mixed-Signal MCUs, Based on ARM® Cortex-M4™ with best-in-class Enablement



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New K-Series devices

- New K10 Sub-families – General Purpose
  - K11 adds Cryptography acceleration and Tamper detection to K10
  - K12 adds additional GPIO in some packages, all support a new power mode for complete shutdown (VLLS0 ~300nA)
- New K20 Sub Families – USB Connectivity
  - K21 adds Cryptography acceleration and Tamper detection to K20
  - K22 adds additional GPIO in some packages, all support a new power mode for complete shutdown (VLLS0 ~300nA)

K11/K12/K21/K22D	
CPU Speed	Up to 50MHz
Memory	Up to 512KB flash, 64KB of SRAM
Packages	48LQFP to 121MBGA
Availability	Production Q1 2013

K21/K22F	
CPU Speed	Up to 100MHz or higher – With Floating Point
Memory	Up to 1MB flash, 128KB of SRAM
Packages	64LQFP to 144MBGA
Availability	Production Q2 2013

Differentiator: Hardware Security Modules

- **Features:**
  - Hardware Cryptographic accelerator unit (CAU)
    - Supports DES, 3DES, AES, MD5, SHA-1, and SHA-256
  - Random Number Generator
    - Generates 32-bit random numbers
    - Ensures statistically good data
  - Hardware Tamper Detect
    - 32-bytes of secure storage
    - Independent power supply, POR, and 32 KHz crystal oscillator
    - 4 passive external tamper sources
    - 2 active external tamper sources
    - Integrated frequency, voltage and temperature sensors

- **Key Benefits**
  - Having HW security modules ensures faster response without CPU loading
  - CAU supports all the most popular encryption methods which gives compatibility with different security applications
  - Facilitates generation of FIPS 140 certifiable random numbers
  - HW tamper detect protects against a wide range of physical attacks on hardware system outside MCU

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Kinetis: Security

K10/K20/K30/K40/K50/K60/K70

Flash Security Options:

- User backdoor access disable
- Factory access disable
- Mass erase disable
- Multiple transfers from Flash to config register

Prevent External accesses for reading or programming

Prevents block and security bit erase, and re-programming. Protects against system impersonation

Protects secure system against electrical noise attacks

Memory Protection Unit (MPU):

- 16 areas, supervisor/user (config registers are fully accessible)

Allows “sandboxing”, running software with restricted access permissions

Cryptographic Acceleration Unit (CAU): (K10/20/50/60/70 only)

- Symmetrical crypto
- Hashing functions
- Random Number Generator (RNG)

Reduces CPU loading for cryptographic functions

Facilitates detection of data tampering

Facilitates generation of FIPS140 certifiable random numbers

Enablement:

- Crypto stacks

Facilitates certificate and authentication to a specific MCU

Secure storage:

- 128 bit unique chip identifier

Accelerates basic data integrity checking

Hardware Cyclic Redundancy Check (CRC)

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Kinetis: Security

K10/K20/K60/K70, 50/120/150MHz

Flash Security Options:
- User backdoor access disable
- Factory access disable
- Mass erase disable
- Multiple transfers from Flash to config registers

Protects against a wide range physical attacks on MCU, even during low power modes

Memory Protection Unit (MPU):
- 16 areas, supervisor/user (config registers are fully accessible)

Tamper Detection (with battery backup):
- Integrated sensors –
  - Frequency
  - Voltage
  - Temperature
- 4x passive external tamper sources (inputs)
- 2x active external tamper sources (2x output and input)

Protects against a wide range physical attacks on hardware system outside the MCU

Cryptographic Acceleration Unit (CAU):
- Symmetrical crypto
- Hashing functions
- Random Number

Highly secure firmware verification, with secure firmware upgrade capability

Enablement:
- High Assurance Boot (HAB) with tools
- Crypto stacks

Protected storage of user key or authentication code, may be used as master key to encrypt additional key depository

Secure storage:
- 256 bit user area, erased by tamper
- 128 bit unique chip identifier

Secure Real Time Clock (RTC):
- Monotonic
- Overflow and reprogram protection

Hardware Cyclic Redundancy Check (CRC)

May be used to prevent firmware downgrading

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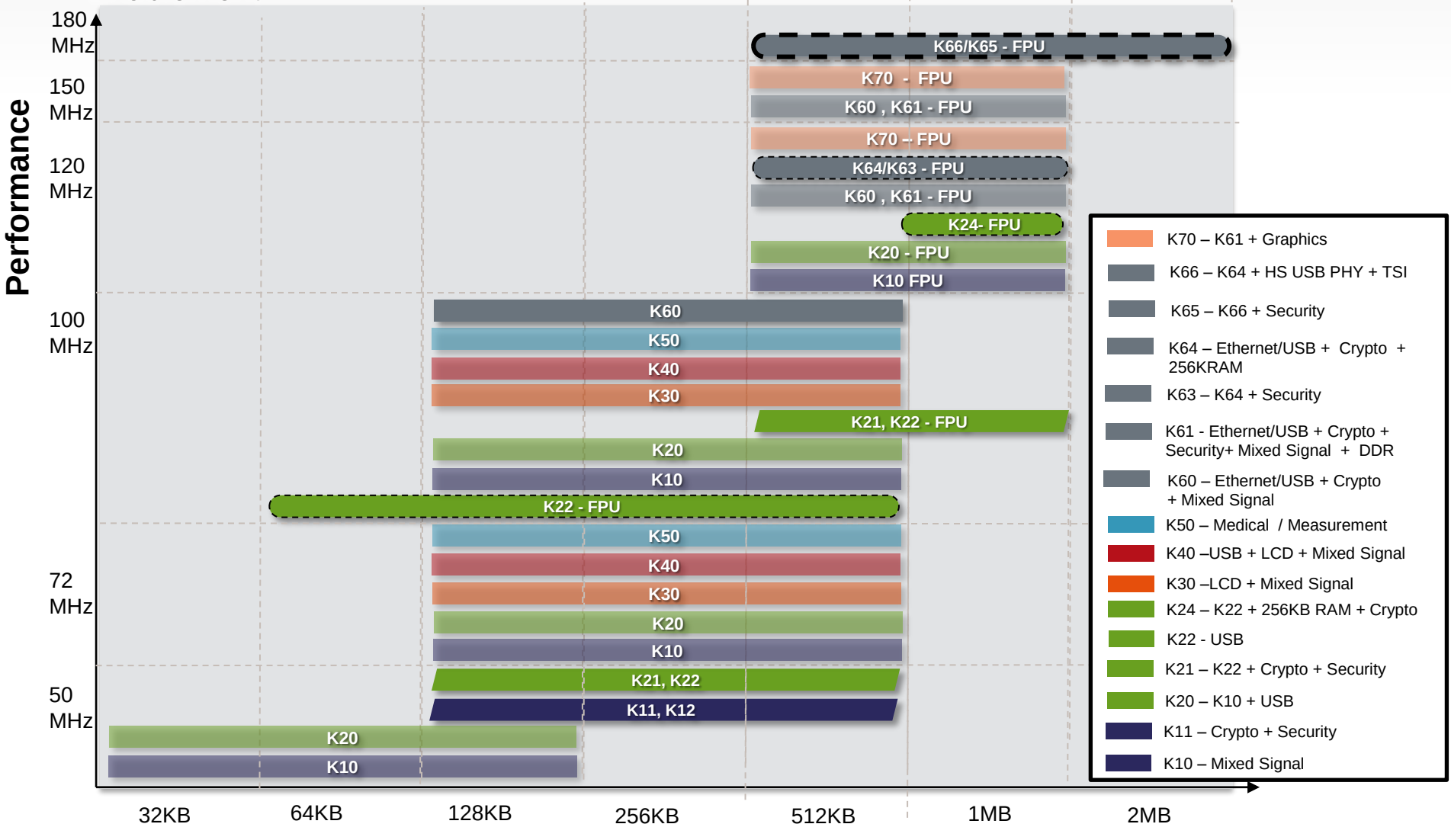
013 Kinetis K Series – Memory Expansion

Scalable, Mixed-Signal MCUs, Based on ARM® Cortex-M4™ with best-in-class Enablement



K24 120MHz Devices (1MB Flash, 256KB SRAM)

Key Features:

Core/System
- Cortex-M4 up to 120MHz with FPU

Memory
- up to 1MB Flash,
- **up to 256KB SRAM**

Communications
- USB OTG FS/LS w/ PHY and USB Vreg
- Multiple serial ports

Analog
- 3 x ACMP,
- 2x 16-bit ADC, Up to 2 x 12-bit DAC
- Analog Vref

Others
- 1.71V-3.6V; -40 to 105°C
- Up to x I/Os (5V tolerant)
- Tamper and Crypto acceleration
- 100 LQFP
  121 MAPBGA (8x8), 144LQFP, 144MBGA

Availability
- Samples: Aug 2013
- Qual/Production: Oct 2013

Core
- Arm Cortex-M4 Up to 120 MHz with FPU
- Debug Interfaces
- DSP
- Interrupt Controller
- Floating Point Unit (sFPU)

System
- Internal and External Watchdogs
- Memory Protection Unit (MPU)
- DMA
- Low-Leakage Wake-Up Unit

Memories
- Program Flash (Up to 1MB)
- SRAM (256KB)
- Serial Programming Interface (EzPort)
- External Bus Interface (FlexBus)

Clocks
- Phase-Locked Loop
- Frequency-Locked Loop
- Low/High Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Random Number Generator
- Cryptographic Acceleration Unit (CAU)

Analog
- Up to 2 x16-bit ADC
- 3 x ACMP
- Up to 2 x 12-bit DAC

Timers
- FlexTimer
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)

Communication Interfaces
- 3xI²C
- 1xI²S
- 6xUARTs
- Secure Digital Host Controller (SDHC)
- 3xSPI
- USB Voltage Regulator
- 1 x USB OTG (LS/FS) + PHY

HMI
- GPIO

K64/63 120MHz Devices (1MB Flash, 256KB SRAM)

Key Features:

Core/System
- Cortex-M4 up to 120MHz with FPU

Memory
- up to 1MB Flash,
- **up to 256KB SRAM**

Communications
- USB OTG FS/LS w/ PHY and USB Vreg
- Multiple serial ports
- Ethernet

Analog
- 3 x ACMP,
- 2x 16-bit ADC, Up to 2 x 12-bit DAC
- Analog Vref

Others
- 1.71V-3.6V; -40 to 105°C
- Up to x I/Os (5V tolerant)
- Tamper and Crypto acceleration
- K64 - 100 LQFP,121 MAPBGA (8x8), 144LQFP, 144MBGA

K63 – 144LQFP, 144MBGA

Availability
- Samples: Aug 2013
- Qual/Production: Oct 2013

Core
- Arm Cortex-M4 Up to 120 MHz with FPU
- Debug Interfaces
- DSP
- Interrupt Controller
- Floating Point Unit (sFPU)

System
- Internal and External Watchdogs
- Memory Protection Unit (MPU)
- DMA
- Low-Leakage Wake-Up Unit

Memories
- Program Flash (Up to 1MB)
- SRAM (256KB)
- Serial Programming Interface (EzPort)
- External Bus Interface (FlexBus)

Clocks
- Phase-Locked Loop
- Frequency-Locked Loop
- Low/High Frequency Oscillators
- Internal Reference Clocks

Security and Integrity
- Cyclic Redundancy Check (CRC)
- Random Number Generator
- Cryptographic Acceleration Unit (CAU)
- DRY ICE

Analog
- Up to 2 x16-bit ADC
- 3 x ACMP
- Up to 2 x 12-bit DAC

Timers
- FlexTimer
- Programmable Delay Block
- Periodic Interrupt Timers
- Low-Power Timer
- Independent Real-Time Clock (RTC)

Communication Interfaces
- 3xI^2C
- 1xI^2S
- 6xUARTs
- Secure Digital Host Controller (SDHC)
- 3xSPI
- USB Voltage Regulator
- 1 x USB OTG (LS/FS) + PHY
- 10/100 Ethernet

HMI
- GPIO

☐ Standard Feature ⬚ Optional Feature

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K61F comparison with K63F

Feature Lists	K61F-Production	K63F-Samples in August
CPU	CM4	Cortex-M4
CPU Frequency	150MHz/120MHz	120MHz
CPU Cache	I-8KB/D-8KB	No
DMA	32ch	16-ch
— EEPROM	16KB	4KB
SRAM	128KB+16KB	256KB
Total RAM	144KB	260KB
FlexRAM	16KB	4KB
Enhanced UART	2	1 (ISO 7816)
UART	4	5 (1 w/FIFO)
DSPI	3	2 w/ 1word FIFO 1 w/ 4 word FIFO
I2C	2	3
I2S	2	1
CAN	2	1
USB OTG LS/FS	1 with PHY	1 with PHY
USB OTG HS	YES	No
USB DCD	YES	Yes-Updated
USB 120mAReg	YES	Yes
Ethernet w /1588	1	1
TSI(Capacitive Touch)	16ch	No
RTC (32KHz Osc, Vbat)	Yes	Yes
16-bit SAR ADC (w temp sense) Total	4	2
PGA	4	No
GPIO w/ dig. Filter	In all I/Os	16 pins
Tamper I/O	8	6
DryICE Features	Standard	Enhanced
Voltage Range	1.71-3.6V	1.71 to 3.6V
Flash Write V	1.71V	1.71 to 3.6V
Temp Range	-40C to 105C	-40 to 105C

K63F increases RAM size to 256KB and keeps similar feature set to K61F

K63F will be highly compatible with K61 (HW and SW)

Enhanced DryICE has updated resistor value and resistor pulsing for passive tamper

K60D-100MHz comparison with K64/63F

Feature Lists	K60D-100MHz-Production	K64/63F-Samples in August
CPU	CM4	Cortex-M4
CPU Frequency	100MHz	120MHz
CPU Cache	No	No
DMA	16-ch	16-ch
— EEPROM	4KB	4KB
SRAM	128KB+4KB	256KB
Total RAM	132KB	260KB
FlexRAM	4KB	4KB
Enhanced UART	1 (ISO 7816)	1 (ISO 7816)
UART	5 (1 w/FIFO)	5 (1 w/FIFO)
DSPI	3	2 w/ 1word FIFO 1 w/ 4 word FIFO
I2C	2	3
I2S	2	1
CAN	2	1
USB OTG LS/FS	1 with PHY	1 with PHY
USB OTG HS	No	No
USB DCD	YES	Yes-Updated
USB 120mAReg	YES	Yes
Ethernet w /1588	1	1
TSI(Capacitive Touch)	16ch	No
RTC (32KHz Osc, Vbat)	Yes	Yes
16-bit SAR ADC (w temp sense) Total	2	2
PGA	2	No
GPIO w/ dig. Filter	In all I/Os	16 pins
Tamper I/O	No	6
DryICE Features	No	Enhanced
Voltage Range	1.71-3.6V	1.71 to 3.6V
Flash Write V	1.71V	1.71 to 3.6V
Temp Range	-40C to 105C	-40 to 105C

K64/63F increases RAM size to 256KB and keeps similar feature set to K60D

K64/63F will be highly compatible with K60 (HW and SW)

Enhanced DryICE has updated resistor value and resistor pulsing for passive tamper

K66/K65 180MHz Devices (2MB Flash, 256KB SRAM)

Key Features:

Core/System
- Cortex-M4 @ 180 MHz with 8KB I-Cache and FPU

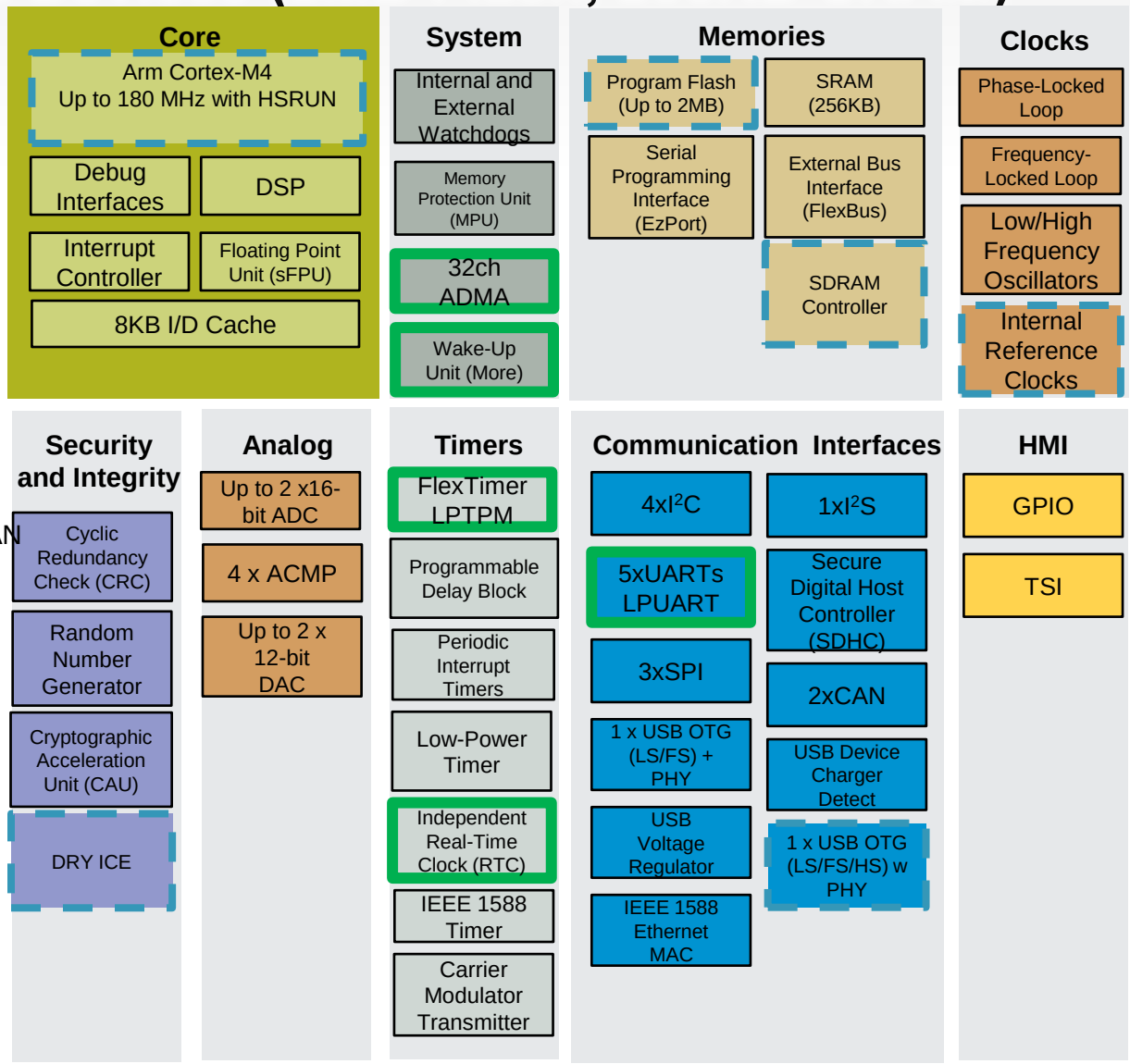
Memory
- up to 2MB Flash,
- up to 256KB SRAM

Communications
- USB OTG FS/LS w/ PHY and USB Vreg.
- USB OTG LS/FS/HS w/PHY
- Ethernet
- Multiple serial ports including dual CAN

Analog
- 4 x ACMP,
- 2x 16-bit ADC, Up to 2 x 12-bit DAC
- Analog Vref

Others
- 1.71V-3.6V; -40 to 105°C
- **up to 105 x I/Os (3V)**
- Tamper and Crypto acceleration
- 144LQFP, 144BGA, 169MBGA

Availability
- Samples: Q4
- Qual/Production: Early Q2 2014



K61F comparison with K65F

Feature Lists	K61F-Production	K63F-Samples in Q3	K65F-Samples in Q4
CPU	Cortex-M4	Cortex-M4	Cortex-M4
CPU Frequency	150MHz/120MHz	120MHz	180MHz
CPU Cache	I-8KB/D-8KB	No	8KB I/D-Cache
DMA	32ch	16-ch	32-ch
— EEPROM	16KB	4KB	4KB
Flash	1MB	1MB	2MB
SRAM	128KB+16KB	256KB	256KB
Total RAM	144KB	260KB	260KB
FlexRAM	16KB	4KB	4KB
Enhanced UART	2	1 (ISO 7816)	1 (ISO 7816)
UART	4	5 (1 w/FIFO)	5 (1 w/FIFO)
DSPI	3	2 w/ 1word FIFO 1 w/ 4 word FIFO	2 w/ 1word FIFO 1 w/ 4 word FIFO
I2C	2	3	3
I2S	2	1	1
CAN	2	1	2
USB OTG LS/FS	1 with PHY	1 with PHY	1 with PHY
USB OTG HS	YES	No	Yes
HS USB PHY	No	No	Yes
USB DCD	YES	Yes-Updated	Yes
USB 120mAReg	YES	Yes	Yes
Ethernet w /1588	1	1	1
TSI(Capacitive Touch)	16ch	No	16ch
RTC (32KHz Osc, Vbat)	Yes	Yes	Yes
16-bit SAR ADC (w temp sense) Total	4	2	2
PGA	4	No	No
GPIO w/ dig. Filter	In all I/Os	16 pins	16 pins
Tamper I/O	8	6	8
DryICE Features	Standard	Enhanced	Enhanced
Secure Storage	32bytes	32bytes	128bytes
Voltage Range	1.71-3.6V	1.71 to 3.6V	1.71 to 3.6V
Flash Write V	1.71 to 3.6V	1.71 to 3.6V	1.71 to 3.6V
Temp Range	-40C to 105C	-40 to 105C	-40 to 105C

K65F adds a new power configuration to support 180MHz operation

K65F increases the secure storage size for the DRYICE

K65F integrates HS USB PHY

K60D comparison with K65F

Feature Lists	K60D-100MHz-Production	K64/63F-Samples in August	K65F-Samples in Q4
CPU	CM4	Cortex-M4	Cortex-M4
CPU Frequency	100MHz	120MHz	180MHz
CPU Cache	No	No	8KB I/D-Cache
DMA	16-ch	16-ch	32-ch (ADMA)
— EEPROM	4KB	4KB	4KB
	512KB	1MB	2MB
SRAM	128KB+4KB	256KB	256KB
Total RAM	132KB	260KB	260KB
FlexRAM	4KB	4KB	4KB
Enhanced UART	1 (ISO 7816)	1 (ISO 7816)	1 (ISO 7816)
UART	5 (1 w/FIFO)	5 (1 w/FIFO)	5 (1 w/FIFO, 1LP)
DSPI	3	2 w/ 1word FIFO 1 w/ 4 word FIFO	2 w/ 1word FIFO 1 w/ 4 word FIFO
I2C	2	3	4
I2S	2	1	1
CAN	2	1	2
USB OTG LS/FS	1 with PHY	1 with PHY	1 with PHY
USB OTG HS	No	No	Yes
HS USB PHY	No	No	Yes
USB DCD	YES	Yes-Updated	Yes
USB 120mAReg	YES	Yes	Yes
Ethernet w /1588	1	1	1
TSI(Capacitive Touch)	16ch	No	16ch
RTC (32KHz Osc, Vbat)	Yes	Yes	Yes
16-bit SAR ADC (w temp sense) Total	2	2	2
PGA	2	No	No
GPIO w/ dig. Filter	In all I/Os	16 pins	16 pins
Tamper I/O	No	6	8
DryICE Features	No	Enhanced	Enhanced
Voltage Range	1.71-3.6V	1.71 to 3.6V	1.71 to 3.6V
Flash Write V	1.71V	1.71 to 3.6V	1.71 to 3.6V
Temp Range	-40C to 105C	-40 to 105C	-40 to 105C

K65F adds a new power configuration to support 180MHz operation

K65F increases the secure storage size for the DRYICE

K65F integrates HS USB PHY

K60 (Ethernet with IEEE1588)													
Sub-Family	Performance (MHz)	Memory				100 LQFP (14x14)	121BGA (8x8)	144LQFP (20x20)	144BGA (13x13)	169BGA (9x9)	256BGA (17x17)	120 VLCSP (5x5)	143 VLCSP (6x6)
		Flash (KB)	FlexNVM (KB)	SRAM (KB)	EEPROM / FlexRAM (KB)								
K60N	100	256	-	64		✓	✓	✓	✓				
	100	512	-	128		✓	✓	✓	✓			✓	
	120	1024	-	128				✓	✓				
	150	1024	-	128				✓	✓				
K60X	100	256	256	64	4	✓	✓	✓	✓				
	120	512	512	128	16			✓	✓				
	150	512	256	128	16			✓	✓				
K61N	120	1024	-	128					✓		✓		✓
	150	1024	-	128					✓		✓		
K61X	120	512	256	128	16				✓		✓		
	150	512	256	128	16				✓		✓		
K64N	120	1024	-	256		✓	✓	✓	✓				
K64X	120	512	128	256	4	✓	✓	✓	✓				
K63N	120	1024	-	256				✓	✓				
K63X	120	512	128	256	4			✓	✓				
K66N	180	2048	-	256				✓	✓				
K66X	180	1024	256	256	4			✓	✓				
K65N	180	2048	-	256						✓			
K65X	180	1024	256	256	4					✓			

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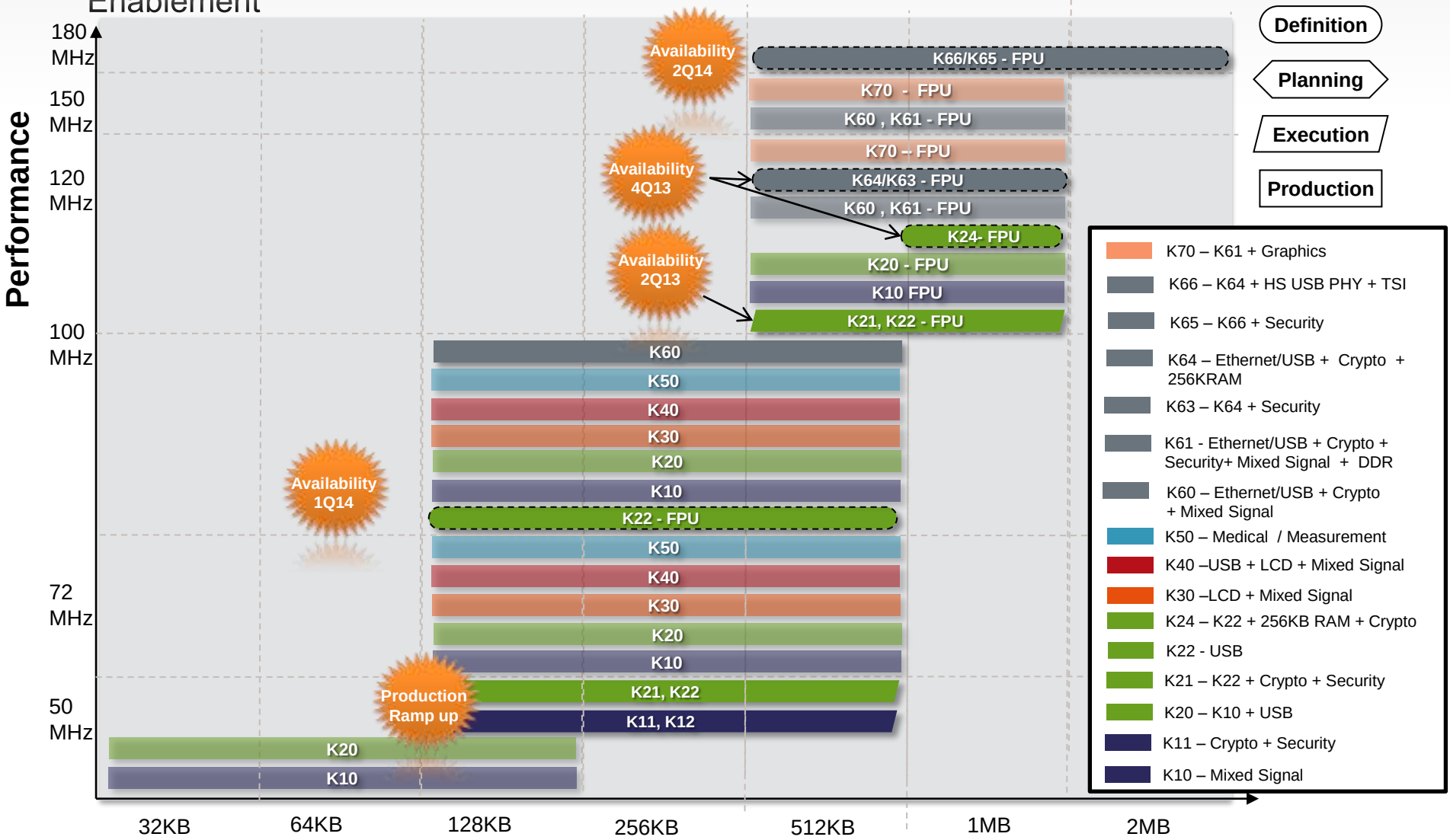
013 Kinetis K Series Roadmap FPU Expansion

Scalable, Mixed-Signal MCUs, Based on ARM® Cortex-M4™ with best-in-class Enablement



K22s – 512K/256K Flash – 120MHz

Key Features:

Core/System
- **Cortex-M4** @ 120MHz / FPU

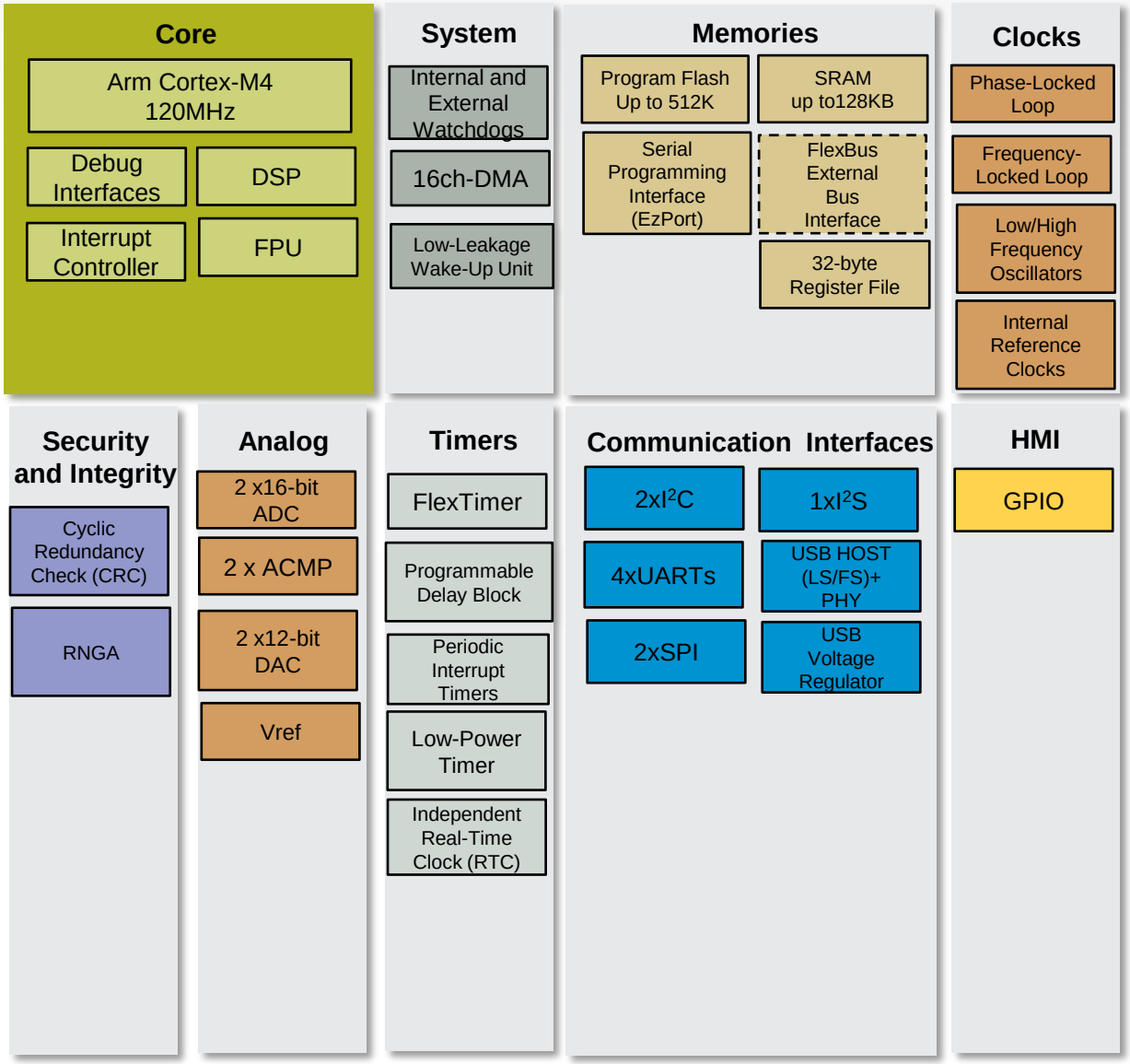
Memory
- up to 512KB Flash,
- up to 128KB SRAM
- FlexBus (External Bus Interface)

Communications
- USB OTG FS/LS
- USB Vreg.
- Multiple serial ports

Analog
- 2 x16-bit ADC
- Up to 2 x12-bit DAC
- 2 x ACMP
- Voltage Reference

Timers
- up to 2x8ch FTM (PWM)
- 2x2ch FTM (PWM/Quad Dec.)
- Low Power Timer
- RTC with independent Vbat. supply

Others
- Up to TBD I/Os
- 6 high-drive I/Os (20mA) – SPI/I2C
- 1.71V-3.6V; -40 to 105oC



Standard Feature Optional Feature

121BGA

K22s – 128K Flash – 100MHz

Key Features:

Core/System
- Cortex-M4 @ 100MHz / FPU

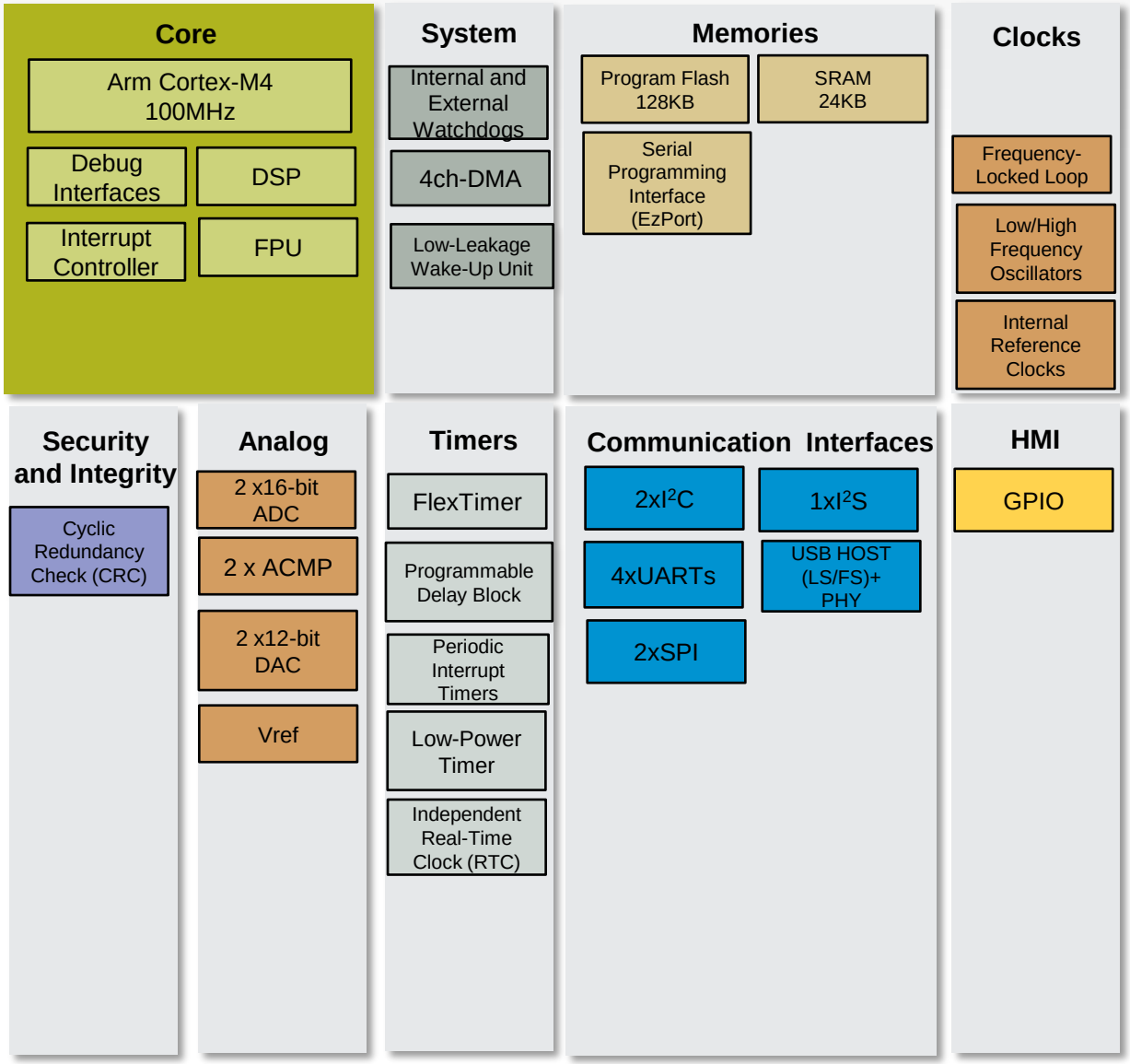
Memory
- 128KB Flash,
- 24KB SRAM

Communications
- USB OTG FS/LS
- Multiple serial ports

Analog
- 2 x16-bit ADC
- 1 x12-bit DAC
- 2 x ACMP
- Voltage Reference

Timers
- 1x8ch FTM (PWM)
- 2x2ch FTM (PWM/Quad Dec.)
- Low Power Timer
- RTC with independent Vbat. supply

Others
- Up to TBD I/Os
- 6 high-drive I/Os (20mA) – SPI/I2C
- 1.71V-3.6V; -40 to 105oC



121BGA Standard Feature Optional Feature

K22s -100/120MHz Part Numbers

MC Partnumber	Max. Freq.	Pin Count	Package	Flash	SRAM	Flex.Bus	DMA	USB Vreg	PLL	FTMs	RNGA	DAC	I/O w/ dig. Filters
MK22FN512VMC10	120MHz	121	BGA	512K	128KB	Yes	16-ch	Yes	Yes	2x8ch; 2x2ch	Yes	2	16
MK22FN512VLL10	120MHz	100	LQFP	512K	128KB	Yes	16-ch	Yes	Yes	2x8ch; 2x2ch	Yes	2	16
MK22FN512VLH10	120MHz	64	LQFP	512K	128KB	Yes	16-ch	Yes	Yes	2x8ch; 2x2ch	Yes	2	16
MK22FN512VMP10	120MHz	64	BGA	512K	128KB	Yes	16-ch	Yes	Yes	2x8ch; 2x2ch	Yes	2	16
MK22FN256VMC10	120MHz	121	BGA	256K	48KB	No	16-ch	Yes	Yes	1x8ch; 2x2ch	Yes	1	8
MK22FN256VLL10	120MHz	100	LQFP	256K	48KB	No	16-ch	Yes	Yes	1x8ch; 2x2ch	Yes	1	8
MK22FN256VMP10	120MHz	64	BGA	256K	48KB	No	16-ch	Yes	Yes	1x8ch; 2x2ch	Yes	1	8
MK22FN256VLH10	120MHz	64	LQFP	256K	48KB	No	16-ch	Yes	Yes	1x8ch; 2x2ch	Yes	1	8
MK22FN128VLL10	100MHz	100	LQFP	128K	24KB	No	4-ch	No	No	1x8ch; 2x2ch	No	1	8
MK22FN128VMP10	100MHz	64	BGA	128K	24KB	No	4-ch	No	No	1x8ch; 2x2ch	No	1	8
MK22FN128VLH10	100MHz	64	LQFP	128K	24KB	No	4-ch	No	No	1x8ch; 2x2ch	No	1	8

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Introducing the New Entry-Level Kinetis L Series

Design Made Simple.

Ultra-low Power

Architected for power efficiency, the Kinetis L series takes advantage of ARM's ultra-low-power Cortex-M0+ processor and features peripherals that help you optimize power consumption.

Leading Scalability and Integration

Expanding on well-known features of the Kinetis platform with leading scalability, best-in-class integration with rich analog features and low-power connectivity, the L series redefines entry-level.

Super Simple

It's 32-bit functionality with 8-bit ease-of-use. Built on the new ARM Cortex-M0+ core (the smallest, lowest-power ARM core), the L series simplifies development with an upward migration path to Kinetis K and X series, software reuse and flexible power optimization. And, with a comprehensive enablement bundle including CodeWarrior IDE, MQX RTOS and the ARM support ecosystem, development is simple.

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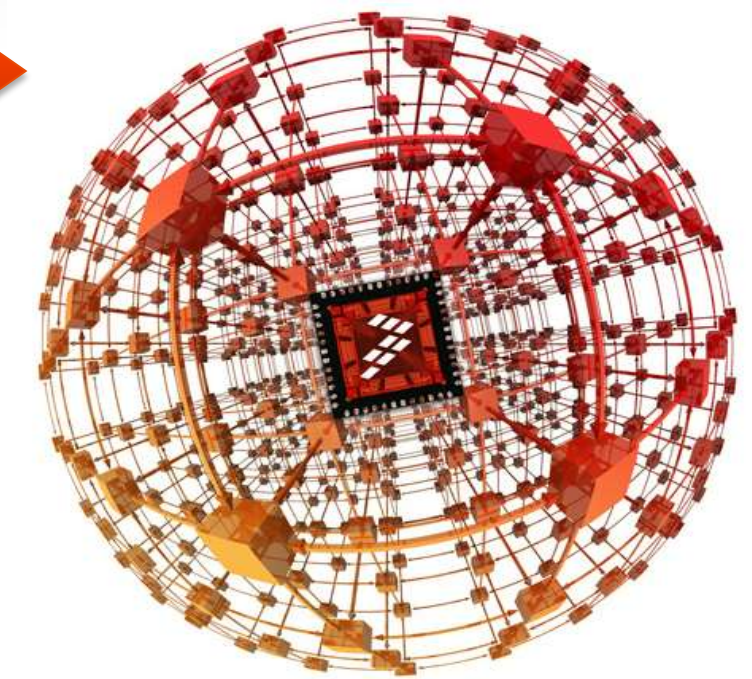
Kinetis L Series:
Enabling Differentiation in Entry-Level Products

32-bit

Energy-efficiency
Class-leading Coremark/mW

Scalability & Integration
Kinetis L to K Series (Cortex M0+ to M4)

Enablement
Freescale bundle + ARM ecosystem



Kinetis L Series
The evolution of the entry-level MCU

8-bit

Ultra Low Static
<1uA

Low Cost
From <$0.50

Ease-of-Use
Freedom Platform, Processor Expert & MCU Solution Advisor

Going Green

Health & Safety

Net Effect

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Kinetis L Series: MCU Families

Common Features
System
ARM Cortex-M0+ Core, 48MHz
Multiple low-power modes, Clock Gating, 1.71V - 3.6V
Operating Temp: -40 to 105°C [1]
Memory
90nm TFS Flash, SRAM
Internal Memory Security/Protection
Analog Peripherals
12/16-Bit ADC
High-Speed Comparators
Serial Interfaces
SCI (Including 1 LPSCI)
SPI, IIC
Timers
Real Time Clock [2]
16bit Low Power TPMs (GP Timer/PWM)
Low Power Timers
32bit Periodic Interrupt Timer

Optional Features									
Family	Flash	SRAM	Key Features						
			USB OTG	Seg. LCD	DMA Cross-Bar	ADC	DAC	I2S	TSI
KL46	128-256KB	16-32KB	√	√	√	16-bit	12-bit	√	√
KL36	64-256KB	8-32KB		√	√	16-bit	12-bit	√	√
KL34	64KB	8KB		√	√	12-bit			
KL26	32-256KB	4-32KB	√		√	16-bit	12-bit	√	√
KL25	32-128KB	4-16KB	√		√	16-bit	12-bit		√
KL24	32-64KB	4-8KB	√		√	12-bit			
KL16	32-256KB	4-32KB			√	16-bit	12-bit	√	√
KL15	32-128KB	4-16KB			√	16-bit	12-bit		√
KL14	32-64KB	4-8KB			√	12-bit			
KL05	8-32KB	1-4KB			√	12-bit	12-bit		√
KL04	8-32KB	1-4KB			√	12-bit			
KL02	8-32KB	1-4KB				12-bit			

[1] Feature not available on CSP packages
[2] For KL02, use software to support

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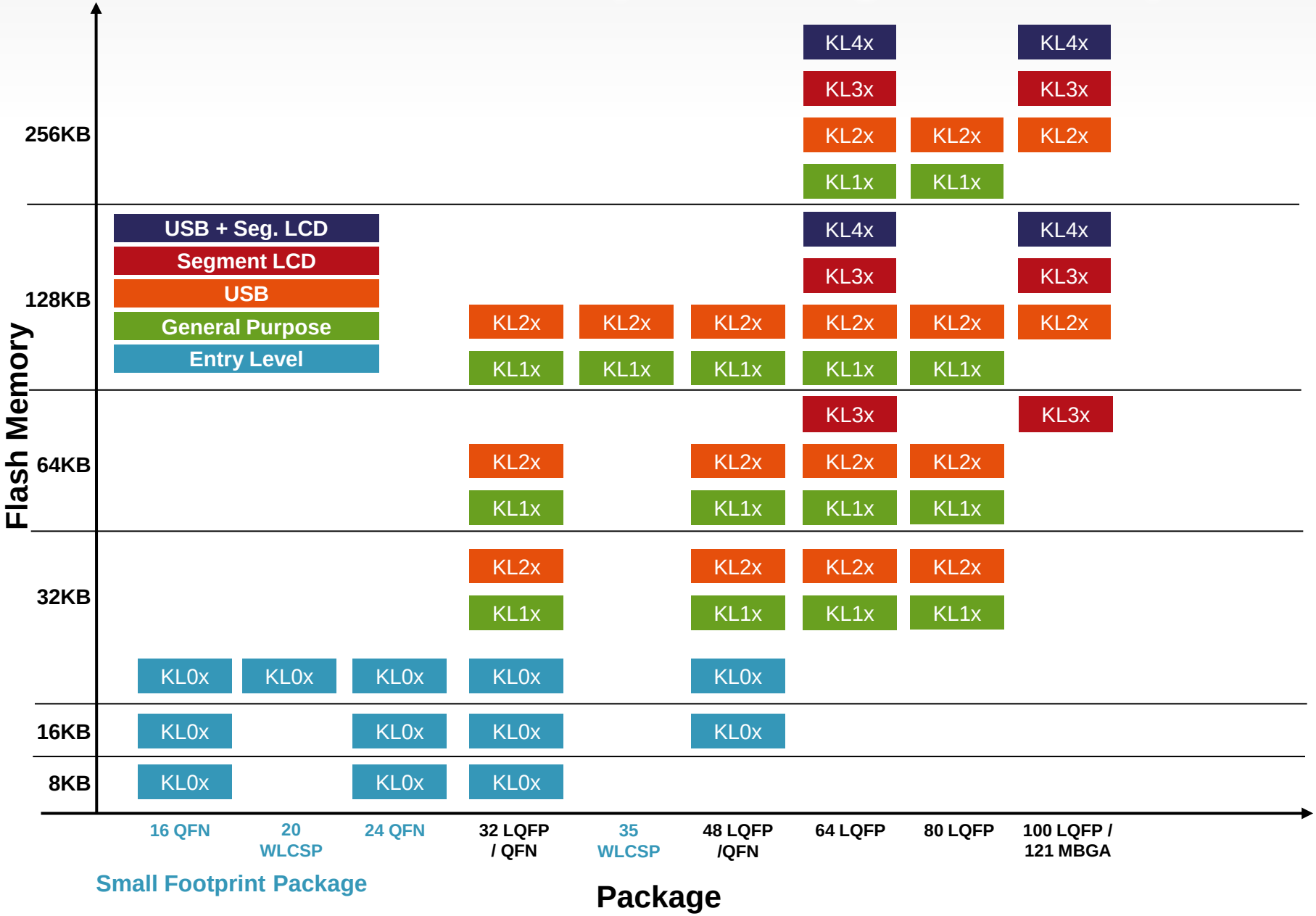
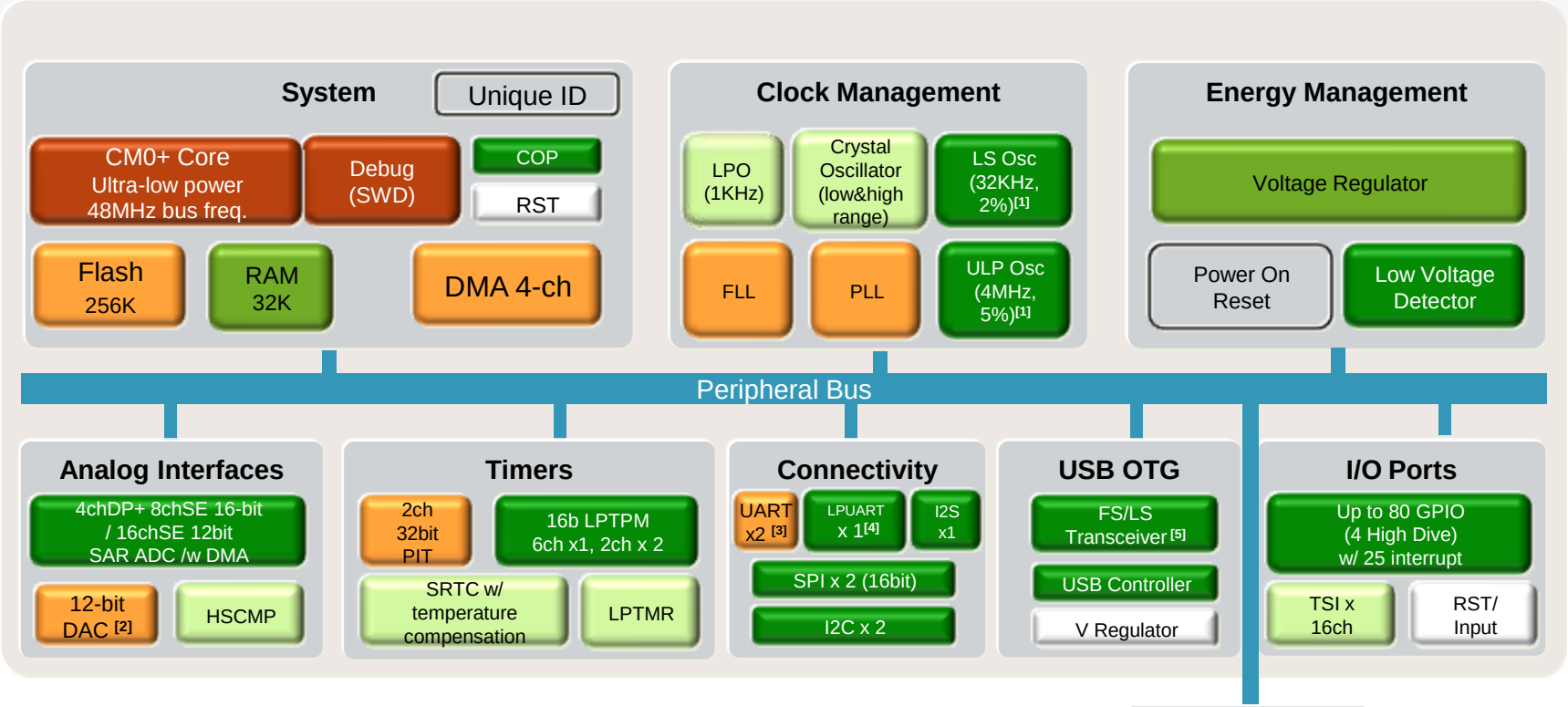
Kinetis L Series: Memory & Package Scalability



...netis L Series: Master Block Diagram



Operation in: Run | Wait | Stop/ VLPS | VLLS 3 | VLLS 1 | VLLS 0

Display

51x8/55x4

100-80-64-48*

CSP*

TBD

48*

121 [6]-64*

*** Under Proposal**

Note: **[1]** 32KHz IRC is only available in Stop mode, while 4MHz IRC is only available in VLPS & Stop modes.
[2] DAC can be functional with constant value in Stop/VLPS mode.
[3] UART can be waken up in Stop/VLPS mode, but cannot receive 1st byte.
[4] **LP**UART can be waken up in Stop/VLPS mode without missing 1st byte.
[5] USB in Stop/VLPS is limited to asynchronous wakeup on resume signaling.
[6] 121 BGA compatible with 21 balls NC.

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Kinetis K/L Series: Packaging

Kinetis K Series Package *Proposed

Kinetis L Series Package *Proposed

Common Packages

32QFN
5 x 5 mm
0.5mm pitch
(K10/20)
(KL0/1/2)

48QFN
7 x 7 mm
0.5mm pitch
(K10/20)
(KL1/2)

32LQFP
7 x 7 mm
0.8mm pitch
(K10/20)
(KL0x)

48LQFP
7 x 7 mm
0.55mm pitch
(K10/20)
(KL0)

64LQFP
10 x 10 mm
0.5mm pitch
(K10/20/30/40/50)
(KL1/2/3/4)

80LQFP
12 x 12 mm
0.5mm pitch
(K10/20/30/40/50)
(KL1/2)

100LQFP
14 x 14 mm
0.5mm pitch
(K10/20/30/40/50/60)
(KL2/3/4)

64MAPBGA
5 x 5 mm
0.5mm pitch
(K10/20)
(KL1*/2*/3*/4*)

121MAPBGA
8 x 8 mm
0.65mm pitch
(K1/2/30/40/50/60)
(KL2/3/4)

Kinetis K Series only

New

56CSP
2.9x3.3x0.56 mm
0.4mm pitch
(K10*/20*)

New

90CSP
3.9x4.4x0.56 mm
0.4mm pitch
(K10*/20*)

New

121CSP
5.3x5.3x0.56 mm
0.4mm pitch
(K10/20/60)

New

143CSP
6.5x5.6x0.56 mm
0.4mm pitch
(K61)

144LQFP
20 x 20 mm
0.5mm pitch
(K10/20/30/40/50/60)

144MAPBGA
13 x 13 mm
1.0mm pitch
(K10/20/30/40/50/60)

256MAPBGA
17 x 17 mm
1.0mm pitch
(K60/70)

Kinetis L Series only

New

20CSP
2x2x0.56 mm
0.4mm pitch
(KL02)

New

25CSP
2.3x2.3x0.56 mm
0.4mm pitch
(KL05*)

New

35CSP
2.55x3x0.56 mm
0.4mm pitch
(KL15*/25*)

New

16QFN
3x3x1 mm
0.5mm pitch
(KL02)

New

24QFN
4 x4x1 mm
0.5mm pitch
(KL0x)

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Breakthrough Power Efficiency

	Kinetis Power Modes	Recovery Time	KL25 Measured Idd @ 3V and 25C
Leading Dynamic Power	RUN	-	83uA/MHz*
Innovative low power process technology (C90TFS)	VLPR	-	39uA/MHz**
Low Power focused Platform Design	WAIT	1.6us	3.88mA @ 48MHz
Next Generation Cortex M0+ core	VLPW	1.6us	112uA @ 4MHz
Asynchronous DMA Wake-up (ADMA)	STOP	1.3us	309uA
Energy-saving peripherals are operational with ADMA feature that can wake-up DMA to perform transfer and return to current mode when complete	VLPS	4.2us	2.4uA
Low Leakage Wake-up Unit	LLS	4.3us	1.7uA
Enables complete shut-down of core logic, including AWIC, further reducing leakage currents in all low power modes	VLLS3	39us	1.3uA
Supports 8 external input pins and 8 internal modules as wakeup sources; extends the low power wake-up capability of some internal peripherals to all power modes.	VLLS1	91us	713nA
Wake-up inputs are activated in LLS or VLLS modes	VLLS0	91us	205nA / 411nA

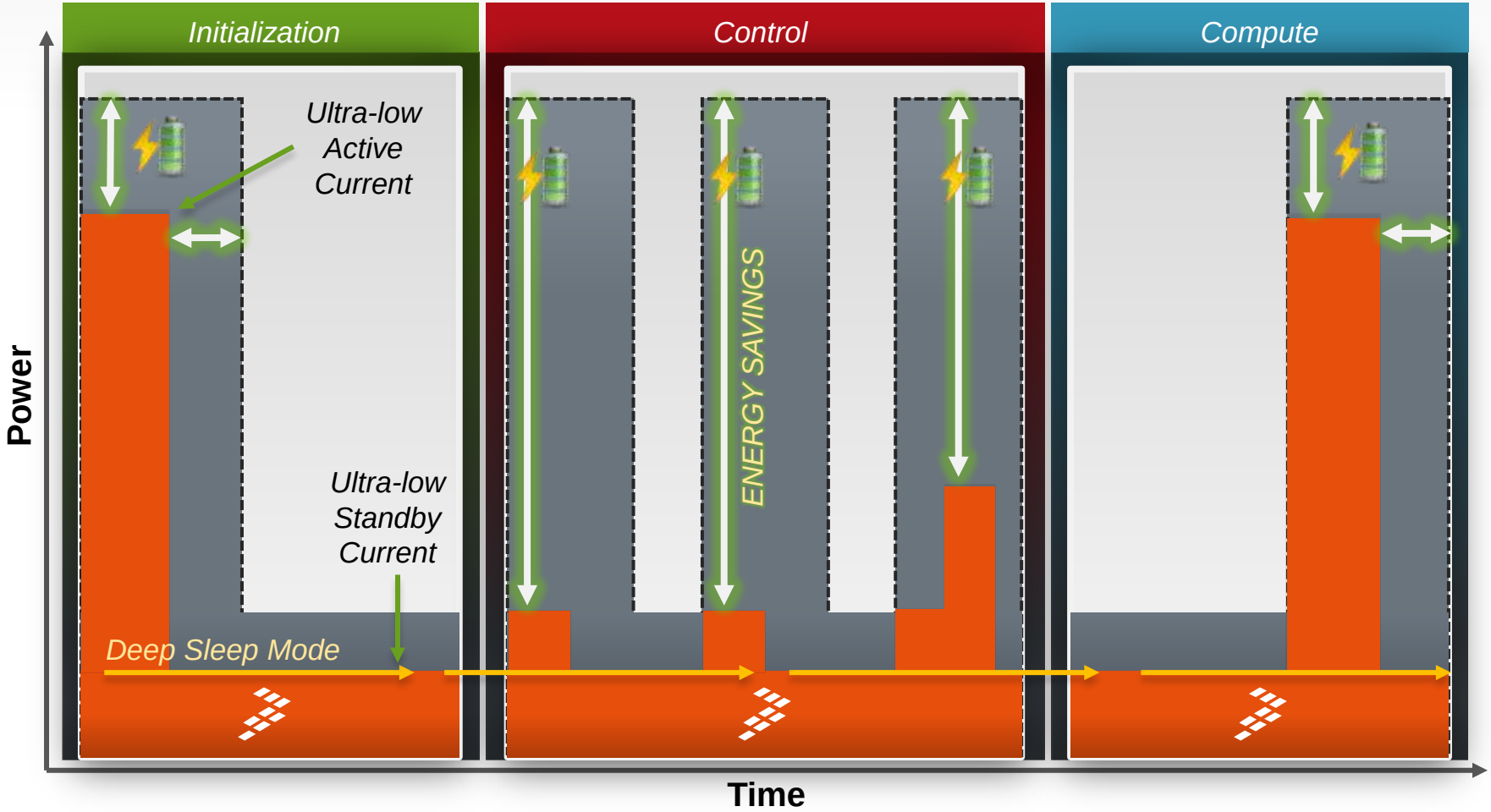
* Compute Operation enabled: 4.0mA @ 48MHz core / 24MHz bus)
** Compute Operation enabled: 156uA @ 4MHz core / 1MHz bus)

Energy Efficiency: Energy = Power x Time

Very Low Active and Standby Power Consumption

Energy Saving Peripherals

Reduced Processing Time



RUN @3V, 48 MHz	83 uA/MHz
VLPR @3V, 4 MHz	39 uA/MHz

VLLS0 Deep Sleep @3V	205 nA
LLS Deep Sleep @3V	1.7 uA

CoreMark/MHz	1.77
LLS Wake-up Time	4.3 us

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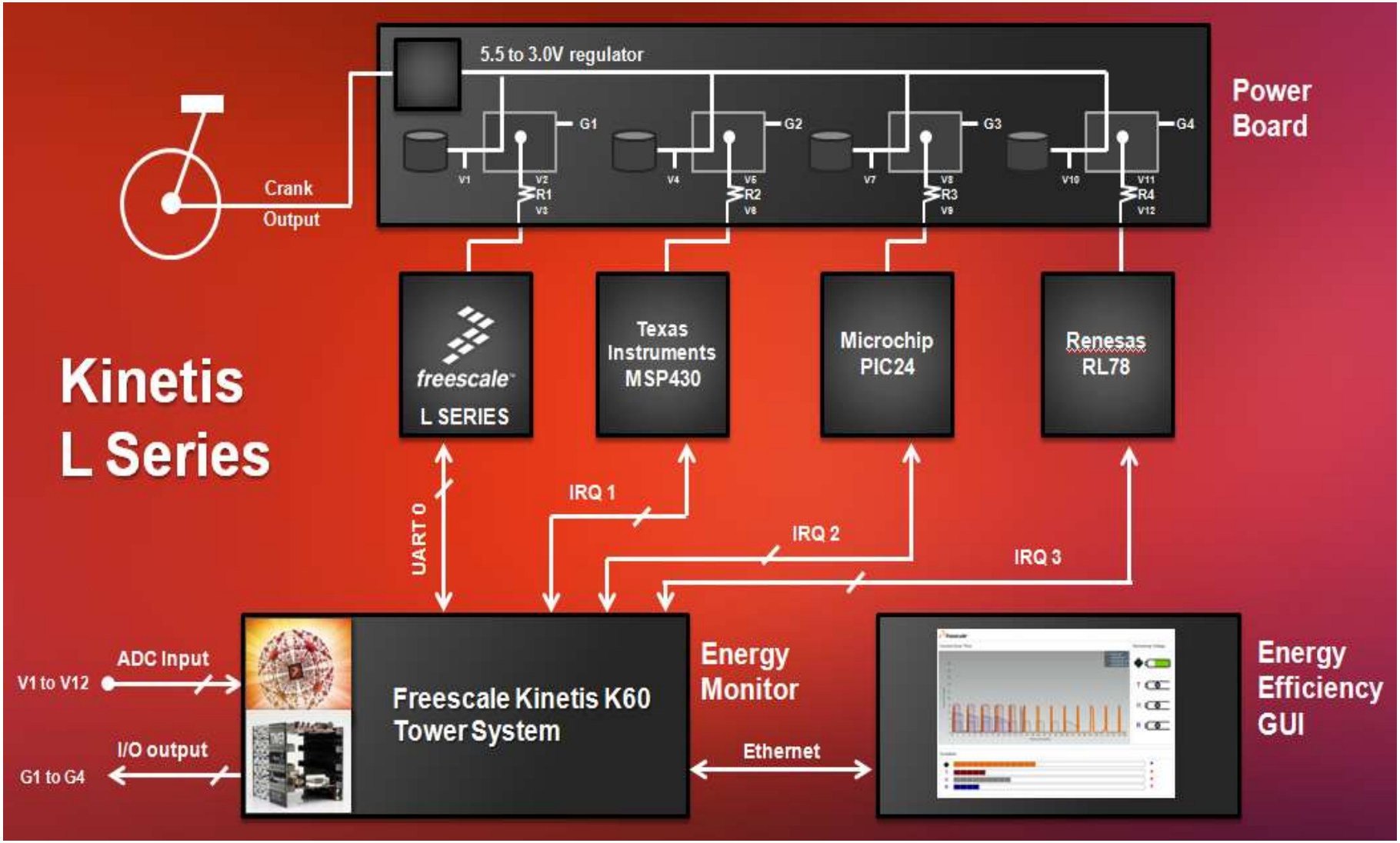
Kinetis L Series Energy-Efficiency Benchmark

Demo: Hardware Overview



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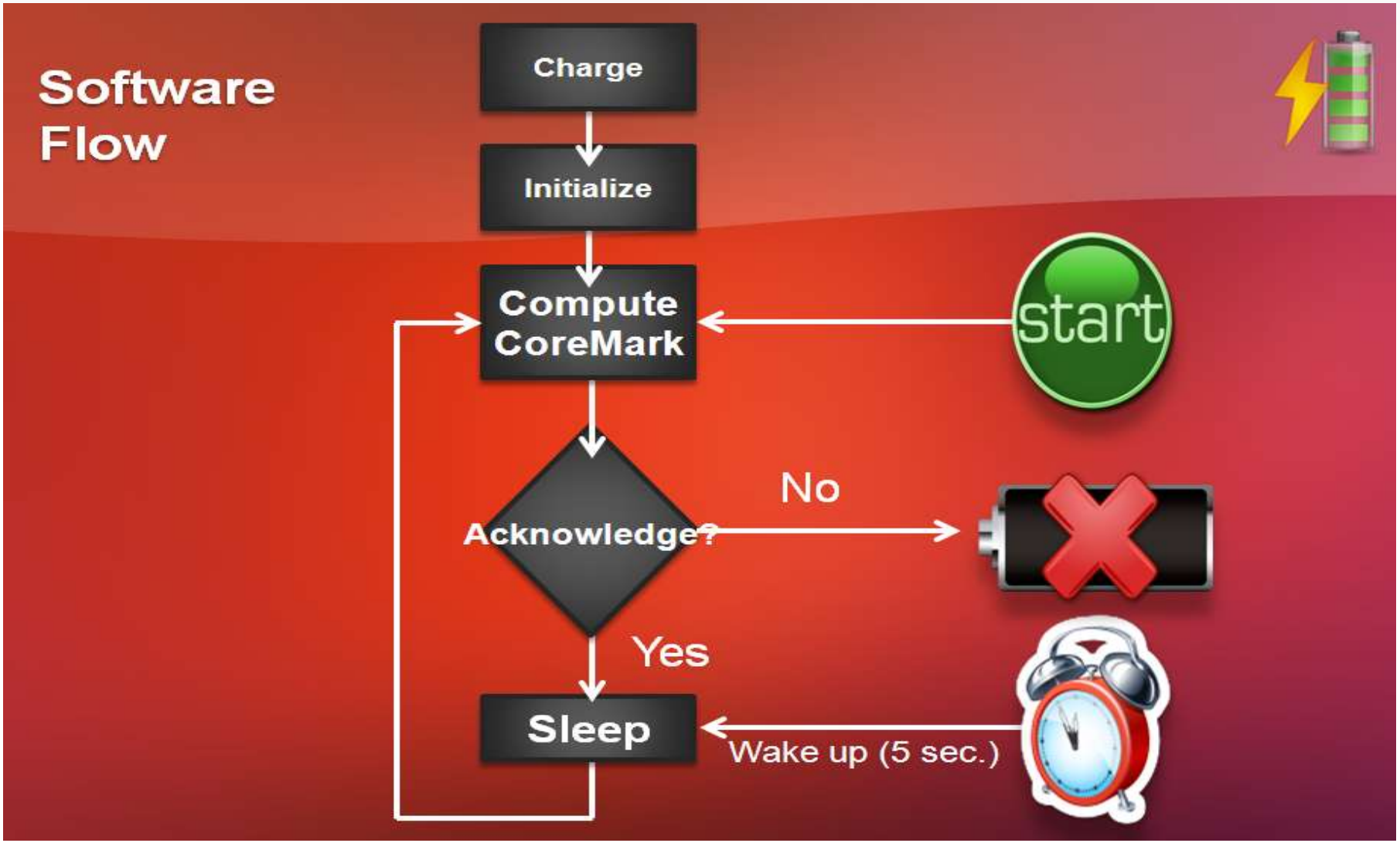
Kinetis L Series Energy-Efficiency Benchmark

Demo: Software Overview



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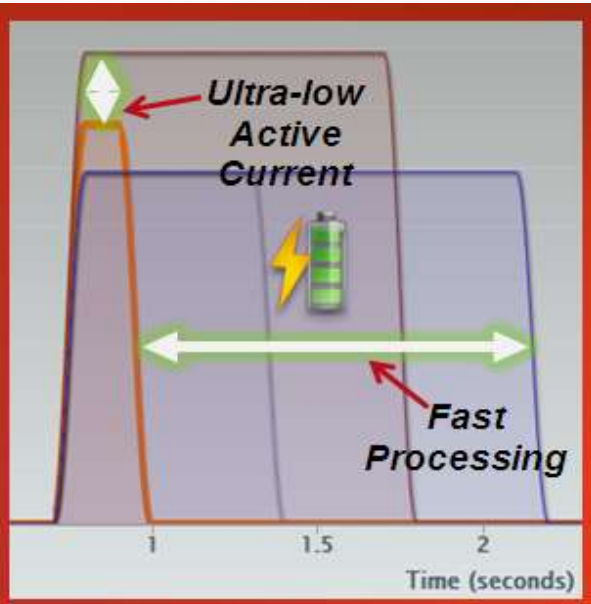
Kinetis L Series MCUs: Energy-Efficiency Benchmark

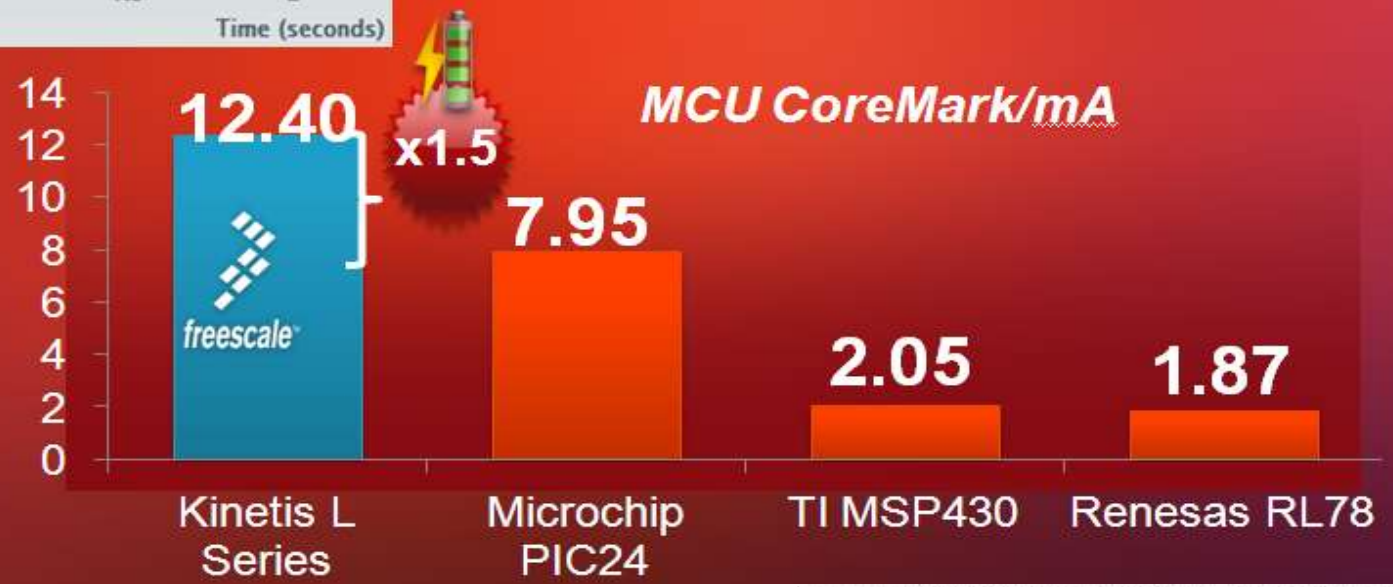
http://www.youtube.com/watch?v=FfsMCwUjNxw

Kinetis L Series Energy-Efficiency Benchmark Demo: Results



Kinetis L Series energy efficiency:

- *Ultra-efficient Cortex-M0+ core*
- *Energy-saving architecture*
- *Flexible ultra-low power modes*



Kinetis L Series: Entry-level Enablement

Hardware

New

Freescale *Freedom Platform*

FRDM-KL25Z

www.freescale.com/FRDM-KL25Z

- Low -cost/power platform for entry-level developers **($12.95 / €10 SRP)**
- Integrates a fully featured debugger, that works with all featured tool chains.

Freescale *Tower System*

TWR-KL25Z48M

www.freescale.com/TWR-KL25Z48M

- Modular, open-source development platform with reusable peripheral modules offering connectivity, analog, graphics LCD and motor control functionality

IDE & Code Generation

Freescale & 3rd party IDEs

- Freescale CodeWarrior v10.3: ***free*** 64KB
- Keil MDK: free 32KB
- IAR EWARM: free 32KB
- Atollic TrueStudio: free 8KB
- GCC ARM Embedded via Launchpad.net

- Additional tool support from Code Red and others in Q412

Freescale *Processor Expert* Code Generator

- ***Free*** software generation tool for device drivers / start-up code
- 7 steps from project creation to debug – dramatically reduces development time
- Available within CodeWarrior or as a standalone plug-in for IAR/Keil/GNU IDEs

CodeWarrior

IAR SYSTEMS

KEIL

Rowley

code_red

atollic

GNU

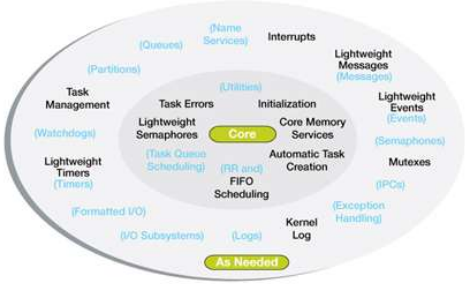
Run-Time Software & Product Selector

New

Freescale *MQX Lite* RTOS

www.freescale.com/mqx

- ***Free***, light-weight MQX kernel customised for small resource MCUs
- Packaged as a Processor Expert component
- Upwards compatible with MQX RTOS



MQX Lite RTOS (MQX RTOS)

Solution Advisor

www.freescale.com/sa

- Web-based interactive MCU selector
- Filters for operating characteristics, packaging, memory configuration & peripherals. Verifies muxing compatibility
- Save, download and print summary reports and pin muxing configurations

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Processor Expert: On-line Training

View in slideshow mode to enable hyperlinks

CodeWarrior version	Microcontroller Driver Suite (Standalone / 3rd party version)

Processor Expert: Introduction (CodeWarrior)

Processor Expert: Working with Components (CodeWarrior)

Processor Expert: The Code Model (CodeWarrior)

Processor Expert: Creating an MQX Lite Project (CodeWarrior)

Processor Expert: An MQX Lite Example (CodeWarrior)

Processor Expert: Exporting and Importing Templates (CodeWarrior)

Processor Expert: Introduction (Driver Suite)

Processor Expert: Working with Components (Driver Suite)

Processor Expert: The Code Model (Driver Suite)

Processor Expert: Creating an MQX Lite Project (Driver Suite)

Processor Expert: An MQX Lite Example (Driver Suite)

Processor Expert: Exporting and Importing Templates (Driver Suite)

Processor Expert: Integrating with IAR Embedded

Processor Expert: Integrating with Keil Microvision

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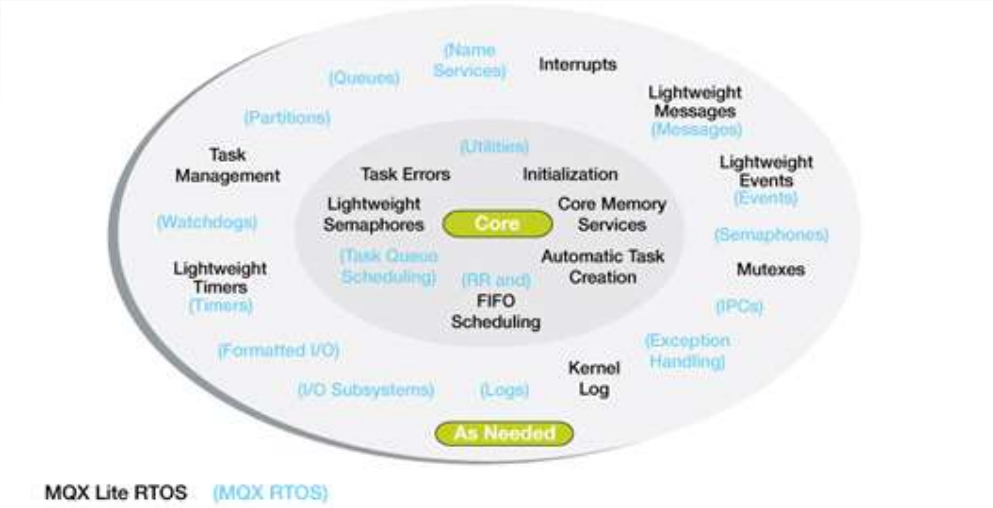
New Freescale MQX Lite RTOS: Overview

www.freescale.com/mqx

- **Very light MQX kernel for resource-limited MCUs**
  - Targeted at the Kinetis L family initially
  - Packaged as a Processor Expert component
- **I/O capability provided by Processor Expert**
  - USB via FSL bare-metal stack, also a Processor Expert component
  - No POSIX-like drivers or file access
- **Programming model allows upward code migration**
  - A true subset of the full MQX RTOS
  - Code built with MQX Lite will move to full MQX RTOS easily
  - Same task templates, same API – some very minor differences
- **Available as a component within the following Freescale s/ware offerings:**
  - Processor Expert software, MCU driver suite – Supports IAR, Keil, and GCC compilers / build chains
  - CodeWarrior Development Studio V10.3



Attribute	MQX RTOS	MQX Lite RTOS
Delivery Mechanism	Traditional installer with full source for Kernel, services and BSPs	Processor Expert (PEx) Kernel and services component, configurable software generated by PEx
I/O Drivers	MQX POSIX compatible drivers with option for using PEx drivers	PEx drivers only
Configurability	User selects needed services from full or lightweight versions	Reduced services available; lightweight options only

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Kinetis ARM Cortex MCU Portfolio (General Purpose)

Performance

ARM Cortex-M4 powered

Kinetis K Series
Industry-first **ARM Cortex-M4** MCU families from 50MHz / 32KB with low power, FlexMemory, mixed-signal and broad connectivity, HMI & security features.

Alpha Samples: Q4 2010
Production: Now

Kinetis L Series
Ultra-low power/cost **ARM Cortex-M0+** MCU families from 32MHz / 8KB with mixed-signal, connectivity & HMI features in low pin-count packages. Compatible with 'K' Series & S08Px
Alpha Samples: Q3 2012
Production: Q4 2012

Kinetis E Series
Robust, low cost **5V ARM Cortex-M0+** MCU families for use in high electrical noise environments. Safety features for high-reliability applications. Compatible with S08Px and 'L' Series
Alpha Samples: Apr 2013
Production: July 2013

ARM Cortex-M0+ powered

Integration

Leading Performance - Low Power - Scalability - Industrial-grade reliability & temp

Freescale Bundled IDE, RTOS & Middleware - Rapid prototyping Platform - Broad ARM Ecosystem Support

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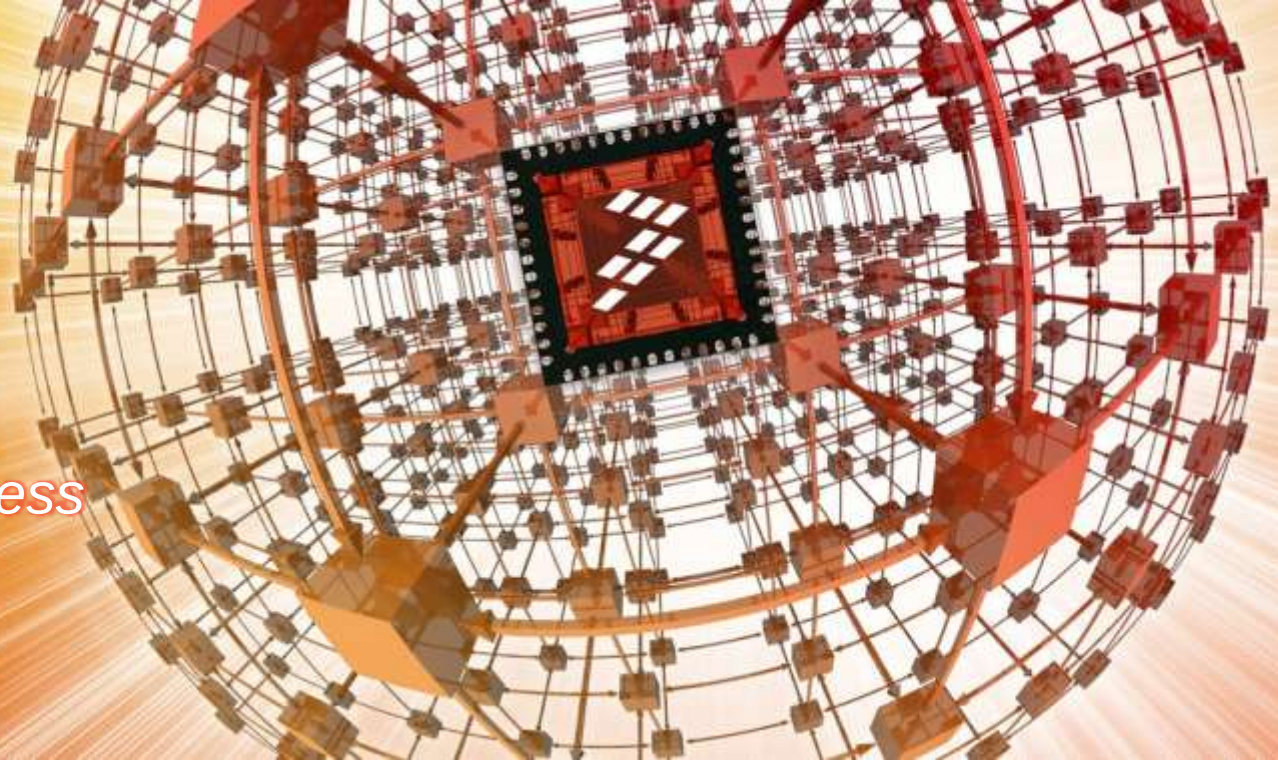

Kinetis E

Strong Robustness
High Efficiency
Low Cost
5V operation

Strong Robustness – EMC/ESD design technology ensure strong noise immunity performance

High Efficiency – Cortex-M0+ core up to 48MHz and 40x more than 8/16-bit MCUs

Low Cost – Optimized for cost-sensitive applications offering low pin count option

Over 50 new devices

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Benefits of Moving from 8/16 -bit to 32-bit ARM Cortex-M0+

8/16-bit

Performance

- Older, slower architectures & technology
- Increased code size/complexity when performing complex math operations

Energy-Efficiency

- Low energy-efficiency

Low Cost

- 6-35kgates
- Variable code density

Ease-of-Development

- Limited addressable memory
- Simplistic interrupt controllers
- Limited scalability (MHz, flash, features)
- Limited ecosystem support

32-bit ARM Cortex-M0+

Performance

- 2x to 40x more than 8/16-bit, 9% more than Cortex-M0
- Fast 32-bit math processing
- Fast single-cycle access to I/O

Energy-Efficiency

- >2x CoreMark/mA than closest 8/16-bit MCU, +30% / CM0

Low Cost

- 12-35kgates
- Excellent code density

Ease-of-Development

- Linear 4GB address space – no need for paging
- Full-featured interrupt controller – simpler s/w architecture
- Huge scalability – h/w and s/w reuse across end products
- Huge ARM ecosystem – off-the-shelf software/tools/training
- Micro Trace Buffer – lightweight, non-intrusive trace

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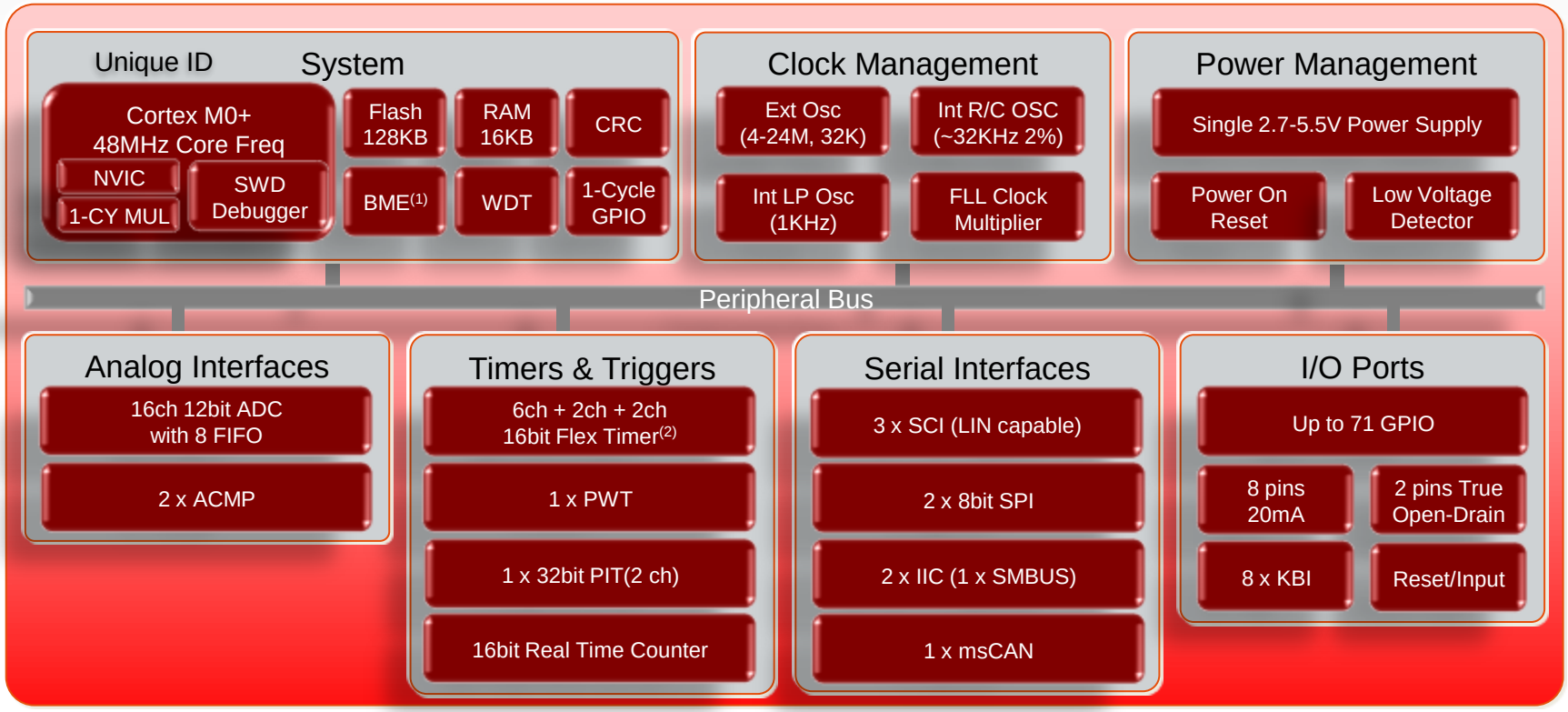
Kinetis E Series: Master Block Diagram



(1) Support bit operation in RAM

(2) Faster timer running 2 x core clock

- Pin compatible within E-series on same package
- Temp: -40~105°C operation

80LQFP(0.65mm pitch);
64QFP (0.8mm pitch); **64LQFP(0.5mm pitch);**
44LQFP (0.8mm pitch);
32LQFP (0.8mm pitch); **24QFN(0.65mm pitch);**
20SOIC(1.27mm pitch); **16TSSOP(0.65mm pitch)**

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Kinetis E Series: MCU Families

Common Features
System
ARM Cortex-M0+ Core, 48MHz [1]
Multiple power modes, Clock Gating, 2.7V – 5.5V
Operating Temp: -40 to 105°C
Clock Management
External OSC, 4~20MHz, 32KHz
Internal OSC, 32KHz, 1KHz
Analog Peripherals
12-Bit ADC
Analog Comparators
Serial Interfaces
SCI
SPI, IIC
Timers
Real Time Clock
16bit Flex timers
32bit Periodic Interrupt Timer

Optional Features									
Family	Speed	Flash	SRAM	Key Features					
				CAN	Seg. LCD	PWT	Fast Timer	ADC	TSI
KE06Z	48MHz	64-128KB	8-16KB	√		√	√	12-bit	
KE04Z128	48MHz	128KB	16KB			√	√	12-bit	
KE04Z64	48MHz	64KB	8KB			√	√	12-bit	
KE04Z8	48MHz	8KB	1KB			√	√	12-bit	
KE02Z	20MHz	16-64KB	2-4KB					12-bit	

[1] 20MHz for KE02

Kinetis Portfolio (Now & in the Future…)

Performance

Availability NOW!

Kinetis L Series
Ultra-low power/cost **ARM Cortex-M0+** MCU families from 48MHz / 8KB with mixed-signal, connectivity & HMI features in low pin-count packages.

Availability NOW!

Kinetis E Series
Robust, 5V **ARM Cortex-M0+ & ARM Cortex-M4** MCU families for use in high electrical noise environments. Safety features for high-reliability applications

Availability NOW!

Kinetis K Series
Industry-first **ARM Cortex-M4** MCU families from 50MHz / 32KB with low power, FlexMemory, mixed-signal and broad connectivity, HMI & security features.

Kinetis X Series
High-performance **ARM Cortex-M4/Mx** MCU families with advanced memory and feature integration for robust, networked industrial and consumer systems

Coming 2014

General Purpose

Segment Focused

Coming 2013 (samples now)

Kinetis W Series
Integrated wireless connectivity **ARM Cortex-M4 and M0+** MCU families with class-leading sub-1 GHz and 2.4 GHz RF transceivers

Coming 2013 (samples now)

Kinetis M Series
High accuracy metrology **ARM Cortex-M0+** MCU families for single chip smart meter implementations.

Kinetis V Series
High efficiency, high speed peripherals **ARM Cortex-M0+ & Cortex-M4** MCU families for use in motor control & power conversion.

Coming 2013 (samples now)

Integration

Leading Performance - Low Power - Scalability - Industrial-grade reliability & temp

Freescale Bundled IDE, RTOS & Middleware - Rapid prototyping Platform - Broad ARM Ecosystem Support

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KV10: 75MHz Cortex-M0+ 32KB Flash

Key Features:

Core/System
- 75MHz **Cortex-M0+** with 4ch DMA
  - Hardware Divide & SqrRoot
  - Bit Manipulation Engine

Memory
- 32KB Flash
- 8KB SRAM

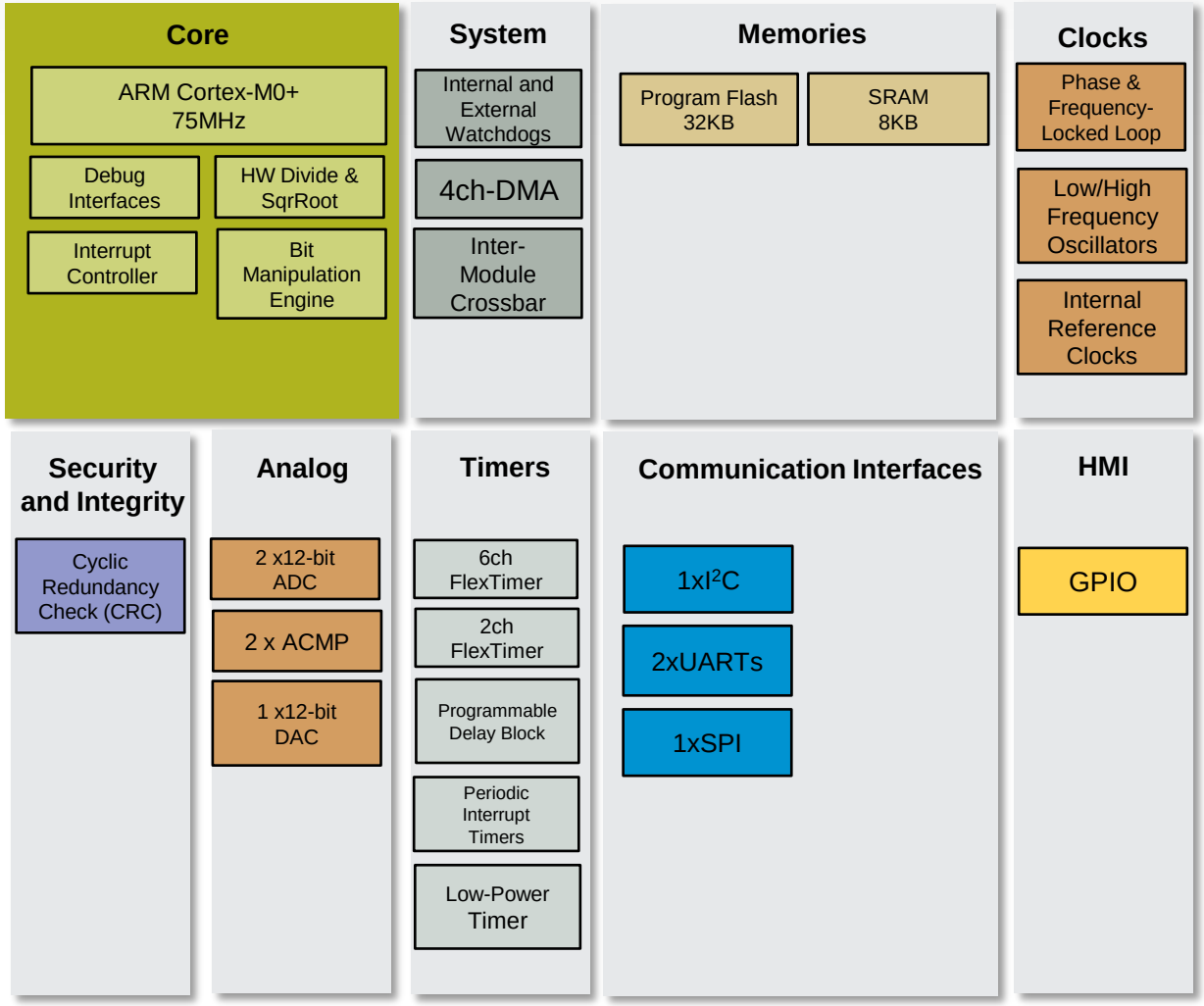
Communications
- Multiple serial ports

Analog
- 2 x 8ch 12-bit ADC
  - 1uS conversion time
- 1 x12-bit DAC
- 2 x ACMP w/ 6b DAC

Timers
- 1x6ch FlexTimer (PWM)
- 1x2ch FlexTimer (PWM/Quad Dec.)
- Programmable Delay Block

Others
- 32-bit CRC
- Intermodule Crossbar Switch
- Up to 35 I/Os
- 1.71V-3.6V; -40 to 105°C

Packages
32QFN, 32LQFP, 48LQFP



KV10s 75MHz: Part Numbers

MC Part Number	Max. Freq.	Pin Count	Package	Flash	SRAM	DMA	PLL	FTMs	DAC
MKV10Z32VLF7	75MHz	48	LQFP	32K	8KB	4-ch	Yes	1x6ch; 1x2ch	1
MKV10Z32VLC7	75MHz	32	LQFP	32K	8KB	4-ch	Yes	1x6ch; 1x2ch	1
MKV10Z32VFM7	75MHz	32	QFN	32K	8KB	4-ch	Yes	1x6ch; 1x2ch	1
MKV10Z16VLF7	75MHz	48	LQFP	16K	8KB	4-ch	Yes	1x6ch; 1x2ch	1
MKV10Z16VLC7	75MHz	32	LQFP	16K	8KB	4-ch	Yes	1x6ch; 1x2ch	1
MKV10Z16VFM7	75MHz	32	QFN	16K	8KB	4-ch	Yes	1x6ch; 1x2ch	1

KV30 – 128K Flash – 100MHz

Key Features:

Core/System
- Cortex-M4 @ 100MHz

Memory
- 128KB Flash,
- 16KB SRAM

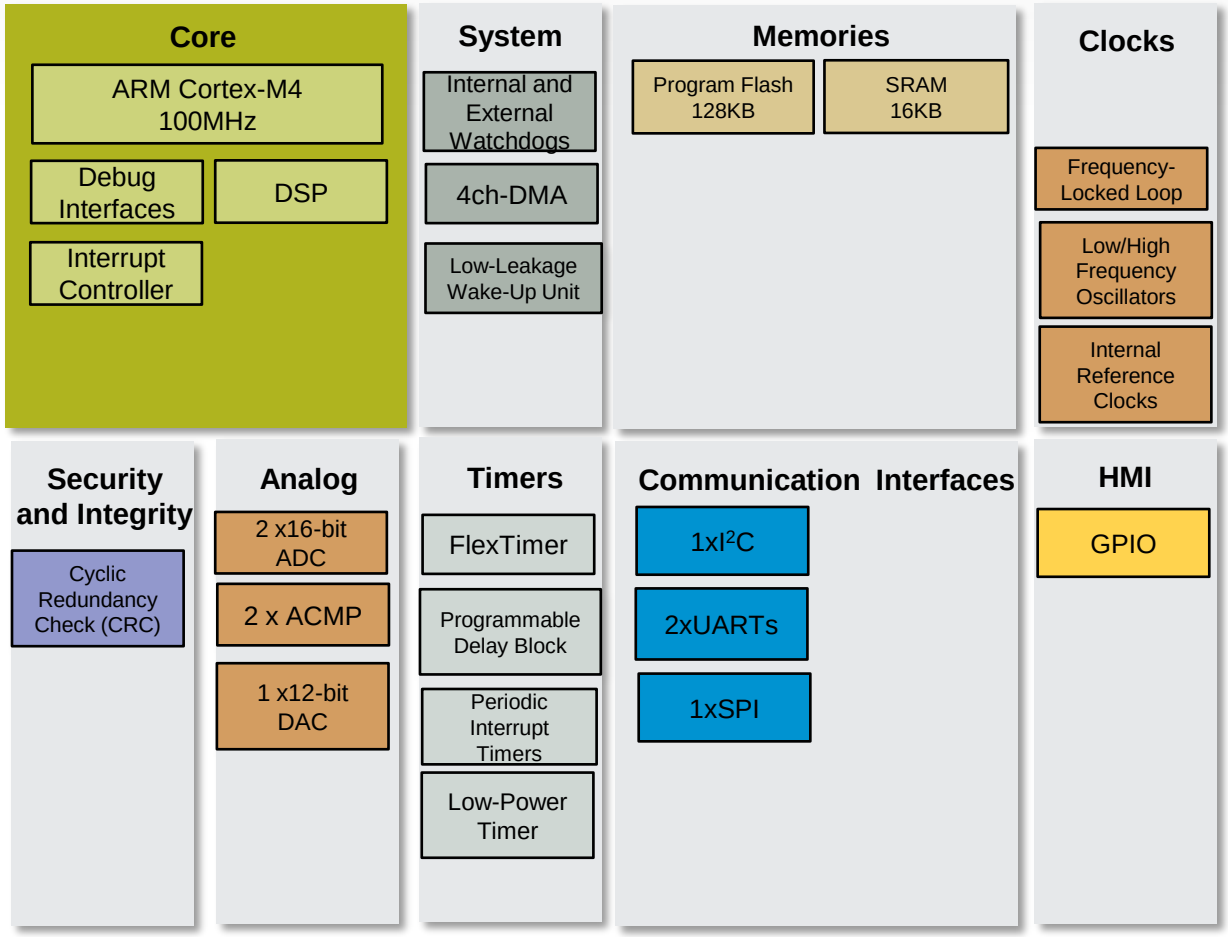
Communications
- Multiple serial ports

Analog
- 2 x16-bit ADC
- 1 x12-bit DAC
- 2 x ACMP

Timers
- 1x6ch FTM (PWM)
- 2x2ch FTM (PWM/Quad Dec.)
- Low Power Timer

Others
- Up to TBD I/Os
- 6 high-drive I/Os (20mA) – SPI/I2C
- 1.71V-3.6V; -40 to 105oC

Packages
32QFN, 48LQFP, 64LQFP



KV30 – 128K Flash – 100MHz / FPU

Key Features:

Core/System
- Cortex-M4 @ 100MHz / FPU

Memory
- 128KB Flash,
- 24KB SRAM

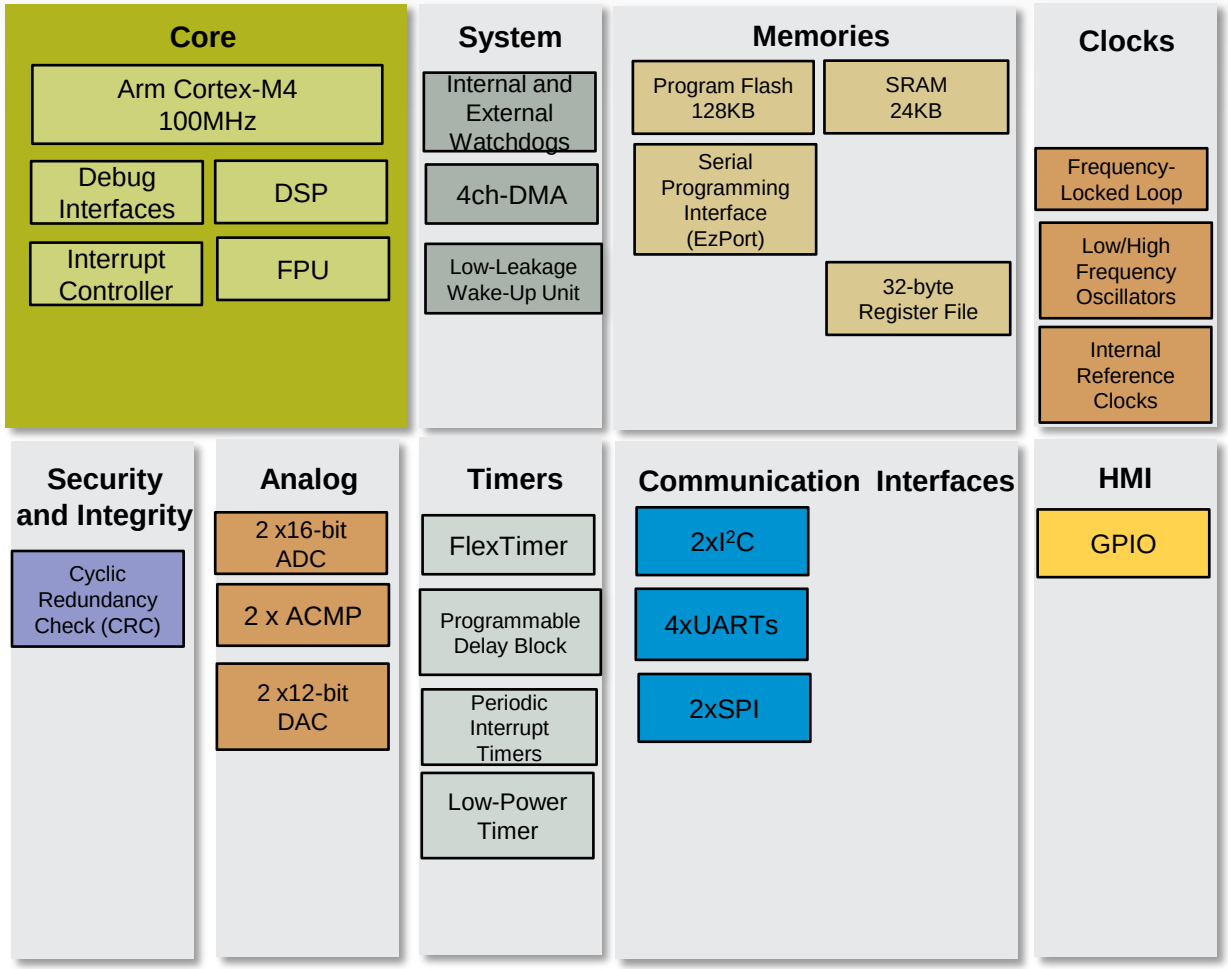
Communications
- Multiple serial ports

Analog
- 2 x16-bit ADC
- 1 x12-bit DAC
- 2 x ACMP

Timers
- 1x8ch FTM (PWM)
- 2x2ch FTM (PWM/Quad Dec.)
- Low Power Timer

Others
- Up to TBD I/Os
- 6 high-drive I/Os (20mA) – SPI/I2C
- 1.71V-3.6V; -40 to 105oC

Packages
64LQFP, 100LQFP



Standard Feature Optional Feature

KV30 – 512K/256K Flash – 120MHz

Key Features:

Core/System
- Cortex-M4 @ 120MHz / FPU

Memory
- up to 512KB Flash,
- up to 128KB SRAM
- FlexBus (External Bus Interface)

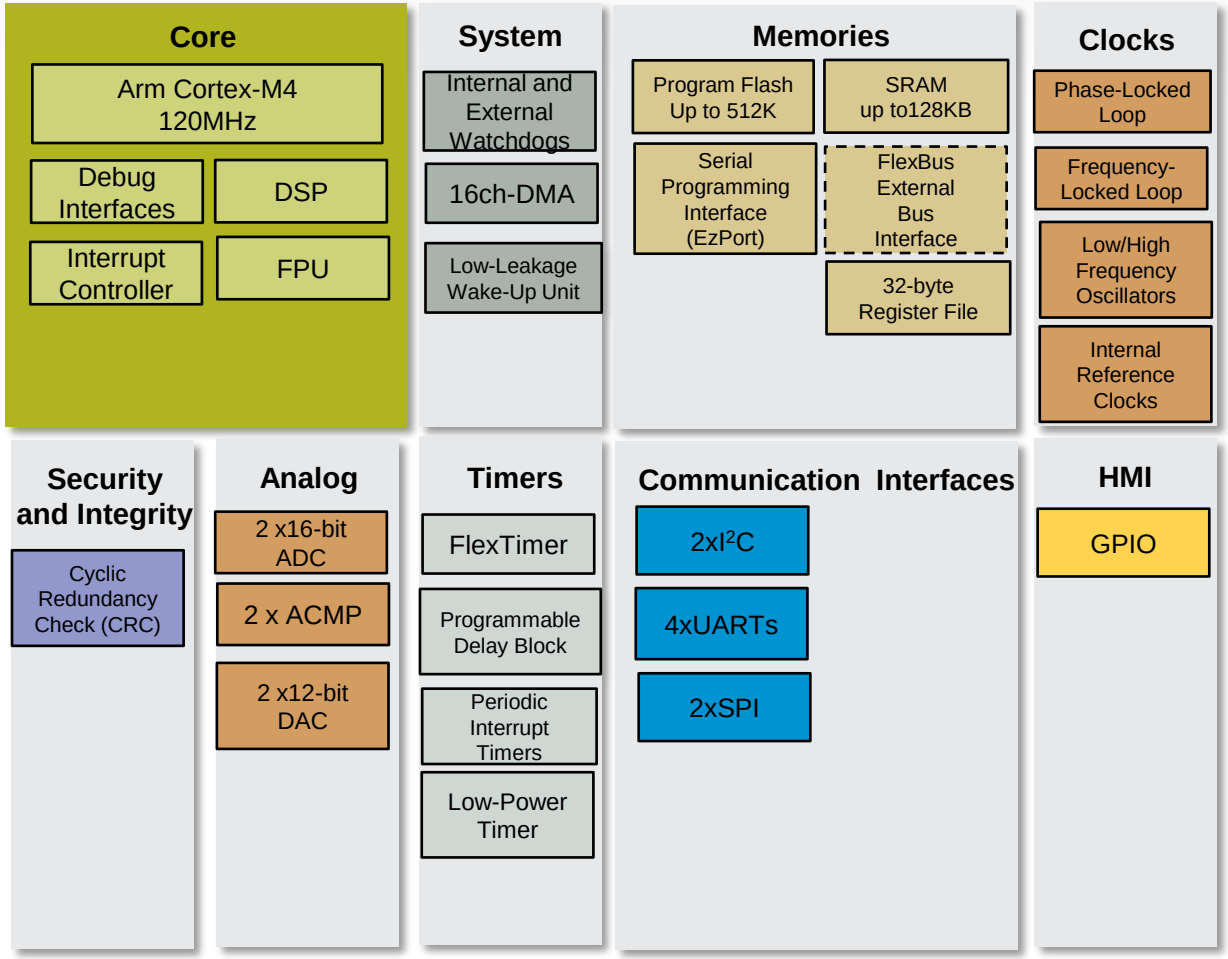
Communications
- Multiple serial ports

Analog
- 2 x16-bit ADC
- Up to 2 x12-bit DAC
- 2 x ACMP

Timers
- up to 2x8ch FTM (PWM)
- 2x2ch FTM (PWM/Quad Dec.)
- Low Power Timer

Others
- Up to TBD I/Os
- 6 high-drive I/Os (20mA) – SPI/I2C
- 1.71V-3.6V; -40 to 105oC

Packages
64LQFP, 100LQFP



Kinetis Portfolio (Now & in the Future…)

Performance

Availability NOW!

Kinetis L Series
Ultra-low power/cost **ARM Cortex-M0+** MCU families from 48MHz / 8KB with mixed-signal, connectivity & HMI features in low pin-count packages.

Availability NOW!

Kinetis E Series
Robust, 5V **ARM Cortex-M0+ & ARM Cortex-M4** MCU families for use in high electrical noise environments. Safety features for high-reliability applications

Availability NOW!

Kinetis K Series
Industry-first **ARM Cortex-M4** MCU families from 50MHz / 32KB with low power, FlexMemory, mixed-signal and broad connectivity, HMI & security features.

Kinetis X Series
High-performance **ARM Cortex-M4/Mx** MCU families with advanced memory and feature integration for robust, networked industrial and consumer systems

Coming 2014

General Purpose

Segment Focused

Coming 2013 (samples now)

Kinetis W Series
Integrated wireless connectivity **ARM Cortex-M4 and M0+** MCU families with class-leading sub-1 GHz and 2.4 GHz RF transceivers

Coming 2013 (samples now)

Kinetis M Series
High accuracy metrology **ARM Cortex-M0+** MCU families for single chip smart meter implementations.

Kinetis V Series
High efficiency, high speed peripherals **ARM Cortex-M0+ & Cortex-M4** MCU families for use in motor control & power conversion.

Coming 2013 (samples now)

Integration

Leading Performance - Low Power - Scalability - Industrial-grade reliability & temp

Freescale Bundled IDE, RTOS & Middleware - Rapid prototyping Platform - Broad ARM Ecosystem Support

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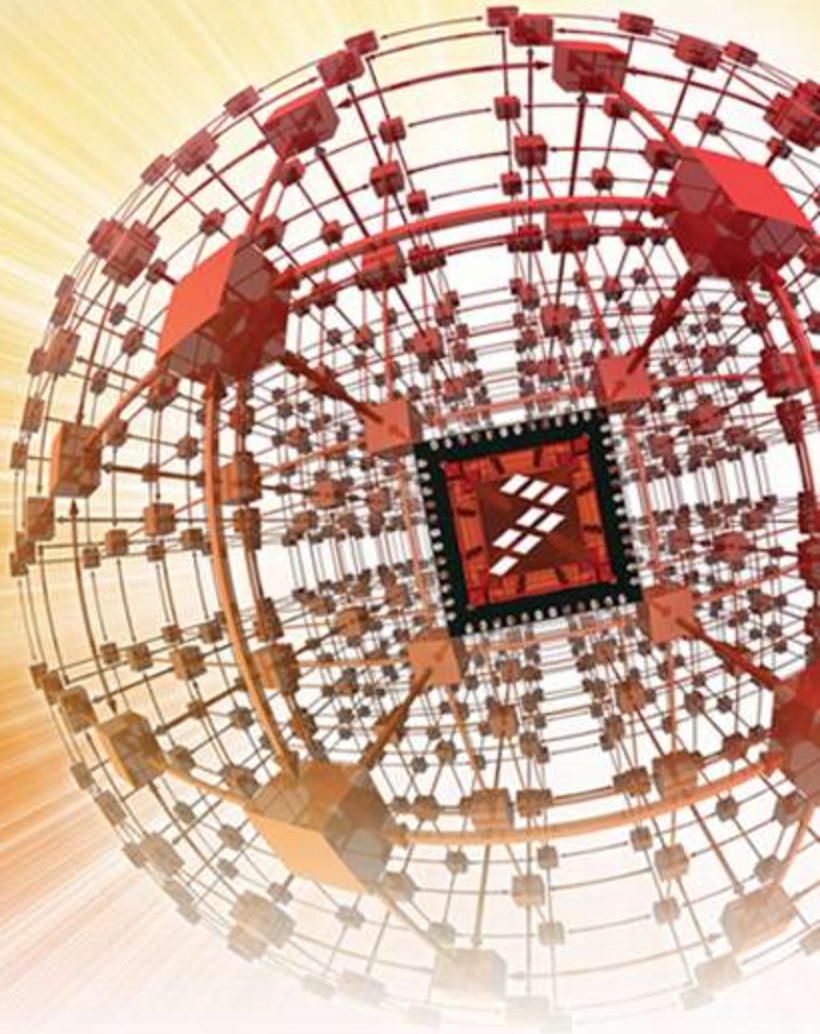
Kinetis M-Series

Smart Metering with High Accuracy Analog

- **Dedicated smart metering peripherals** tailored with regional specifications
- Supports low-cost, highly integrated solutions for one- or two-phase meters with a **high accuracy sigma delta ADC metering front end**
- Address specific **regional needs** including neutral disconnect or split phase for North America and Japan.
- **Full metrology software**, including time or filter based, is provided as well as fast Fourier transform.



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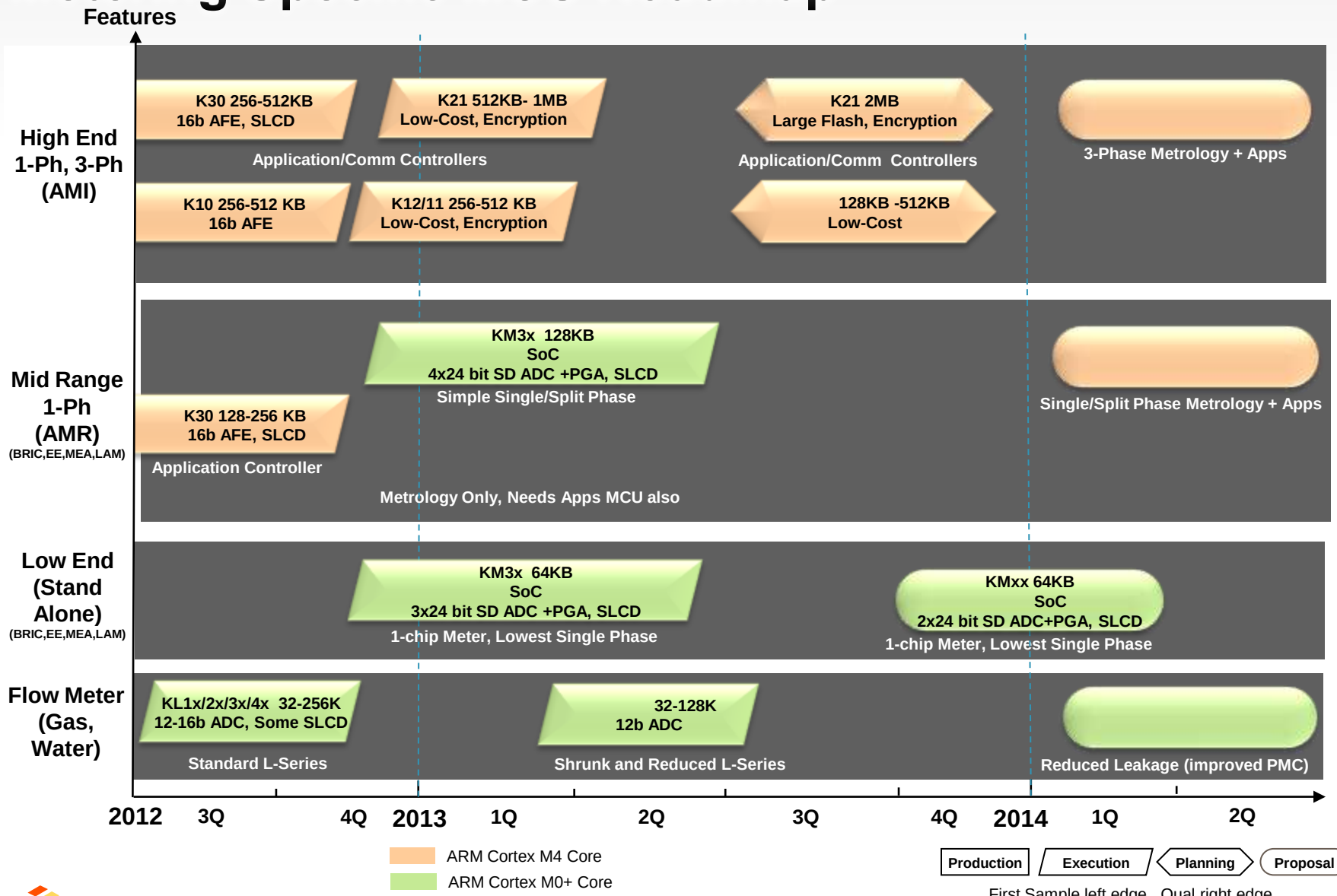
Metering Specific MCU Roadmap



First Sample left edge, Qual right edge

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M1x/KM3x One Pager

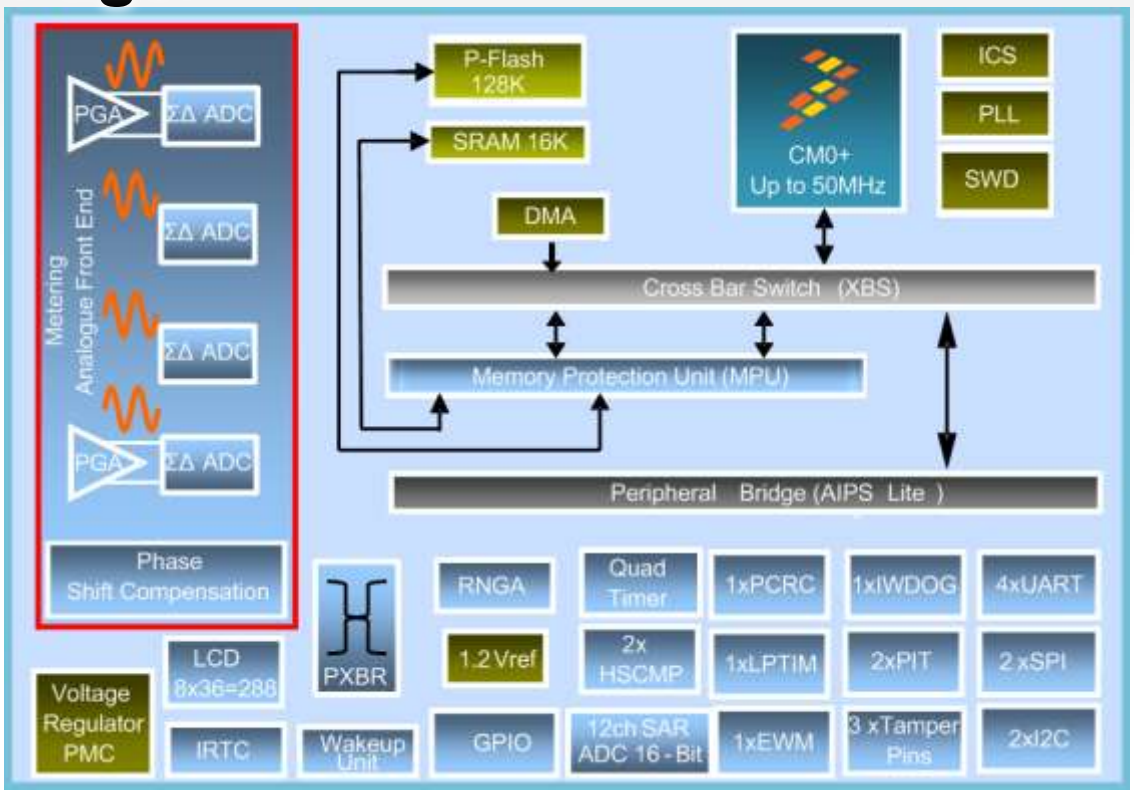
Core
- CM0+ core Up to 50MHz
- Separate FLL post-scalers for IPBus and Core clocks.
- Up to 128 KB Program Flash
- Up to 16 KB SRAM
- Dedicated PLL for ΣΔ modulator clock
- 4ch DMA
- Single 32kHz Crystal operation
  - MHz Crystal Optional

Security & Encryption
- MPU & AIPS
- IRTC w/t tamper detection
- 3 Tamper pins (operating from battery)
- Programmable 16/32-bit CRC
- Random Number Generator (NIST: SP800-90)
- AES Encryption (via software library)

Analog
- 4x24 bit ΣΔ (2xPGA) highly accurate supporting EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23, optimized for shunt sensor (≥50uOhm).
  - 0.1% error in active and reactive energy over a dynamic range of 2000 to 1
- Internal 1.2V reference voltage 10-15ppm/C
- 12-ch 16-bit SAR for auxiliary measurement
- 2x analog comparator

Serial Communications
- 2x SPI
- 4x UART
  - 1 combined with Quad Timer, HSCMP for IR
  - 2 support ISO7816
  - All support flow control
- 2× I2C
- All UARTs and SPIs are 3V compatible while 1 UARTs and 1 SPI are both 3V and 5V compatible (open drain / push pull configuration)

Peripheral XBAR
- Remapping peripheral IOs
- UART selection for IR



Timer/PWM/Clock
- Quad Timer (total 4 universal timers)
- 2x PIT
- 1x Watchdog Timer (windowed, independently clocked)
- 1x EWM (External Watchdog Monitor)
- 1x LPTimer

LCD Display
- Up to 288 segment LCD, up to 8 backplanes

Wakeup Unit
- Group selected GPIOs (16), LPTIM, RTC (+tamper pins) , HSCMP, SCI , Brownout and POR sources to wake up from Power Gated STOP mode

GPIO
- Up to 64 with open drain / push pull, pull up/down
- Up to 8 GPIO with filter
- Support for interruption on any edge

Power
- Power Management
- PMC (Power Manager Control Unit)
- 2.7V to 3.6V Operating voltage with AFE
- 1.71V to 3.6V Operating voltage without AFE
- 1.71V-3.6V IRTC VBAT supply
- 32kHz or 2MHz internal clock source
- 32.768kHz crystal oscillator

Package
- 100 LQFP, 64 LQFP and 44 LGA options
- -40°C ~ +85°C Temp

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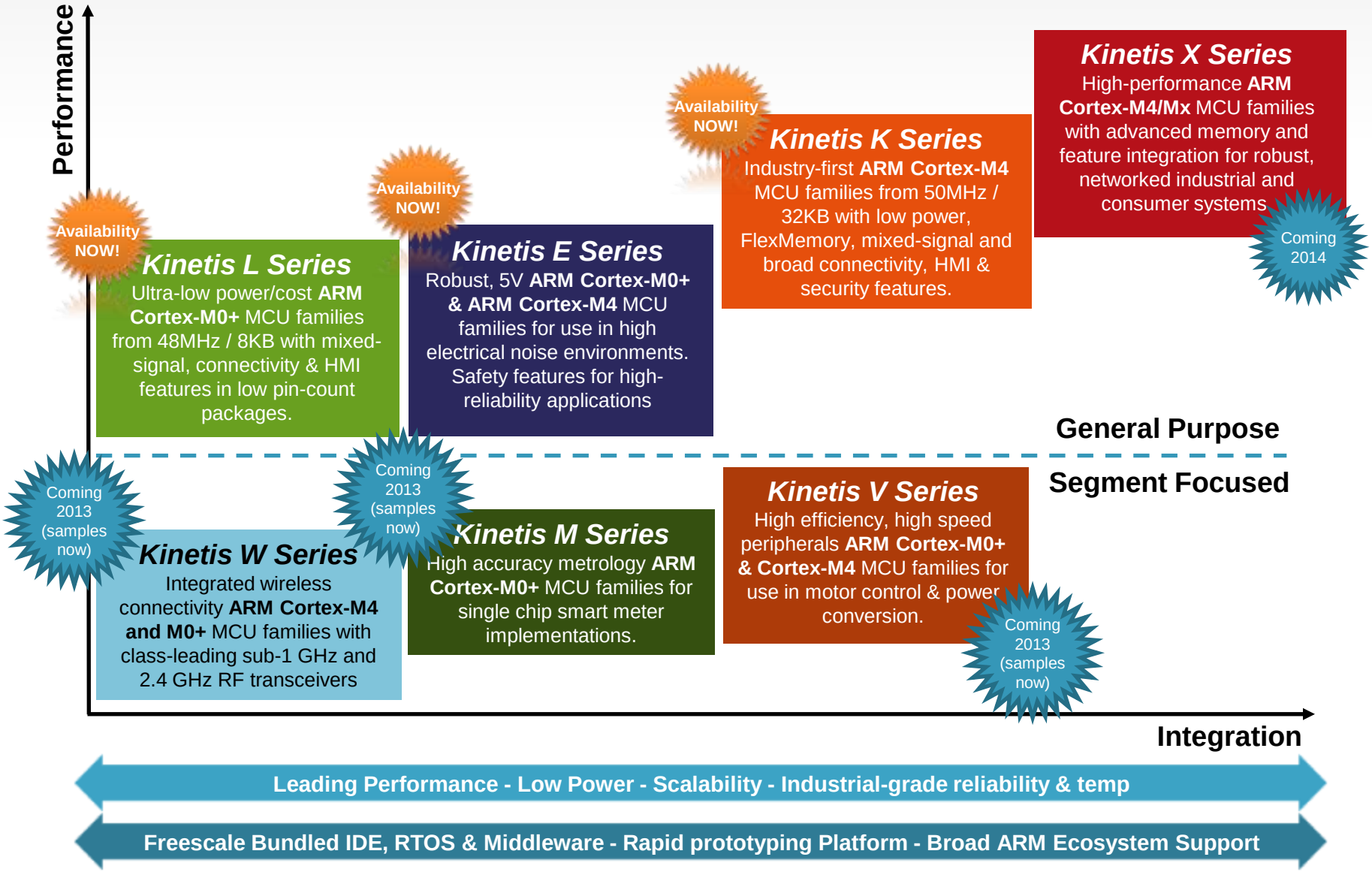
Kinetis Portfolio (Now & in the Future…)



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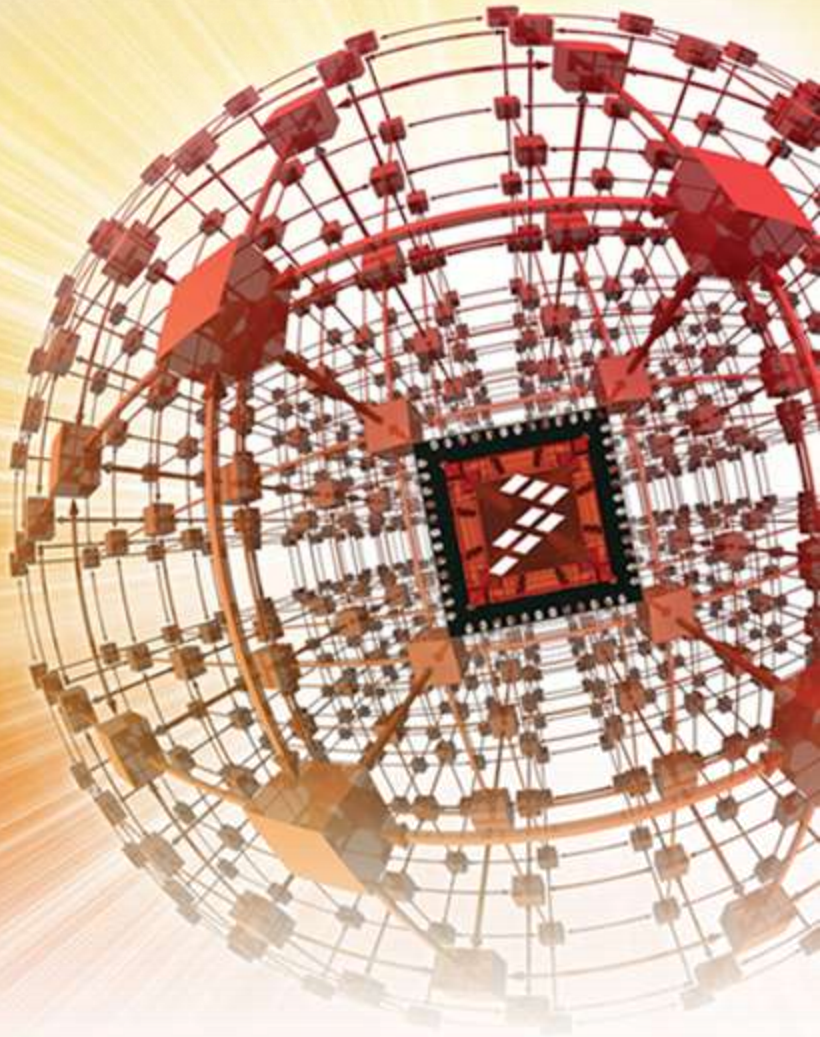
Kinetis W-Series

Integrated Wireless Connectivity

- **Integrates class-leading sub-1 GHz and 2.4 GHz RF transceivers** with Cortex™ core
- Robust feature sets for reliable, **secure and low-power** embedded wireless solutions
- **Optimized for wireless**, providing the right mix of performance, integration, connectivity and security
- Sub 1-GHz or 2.4 GHz wireless, simple **point-to-point or full mesh networking**



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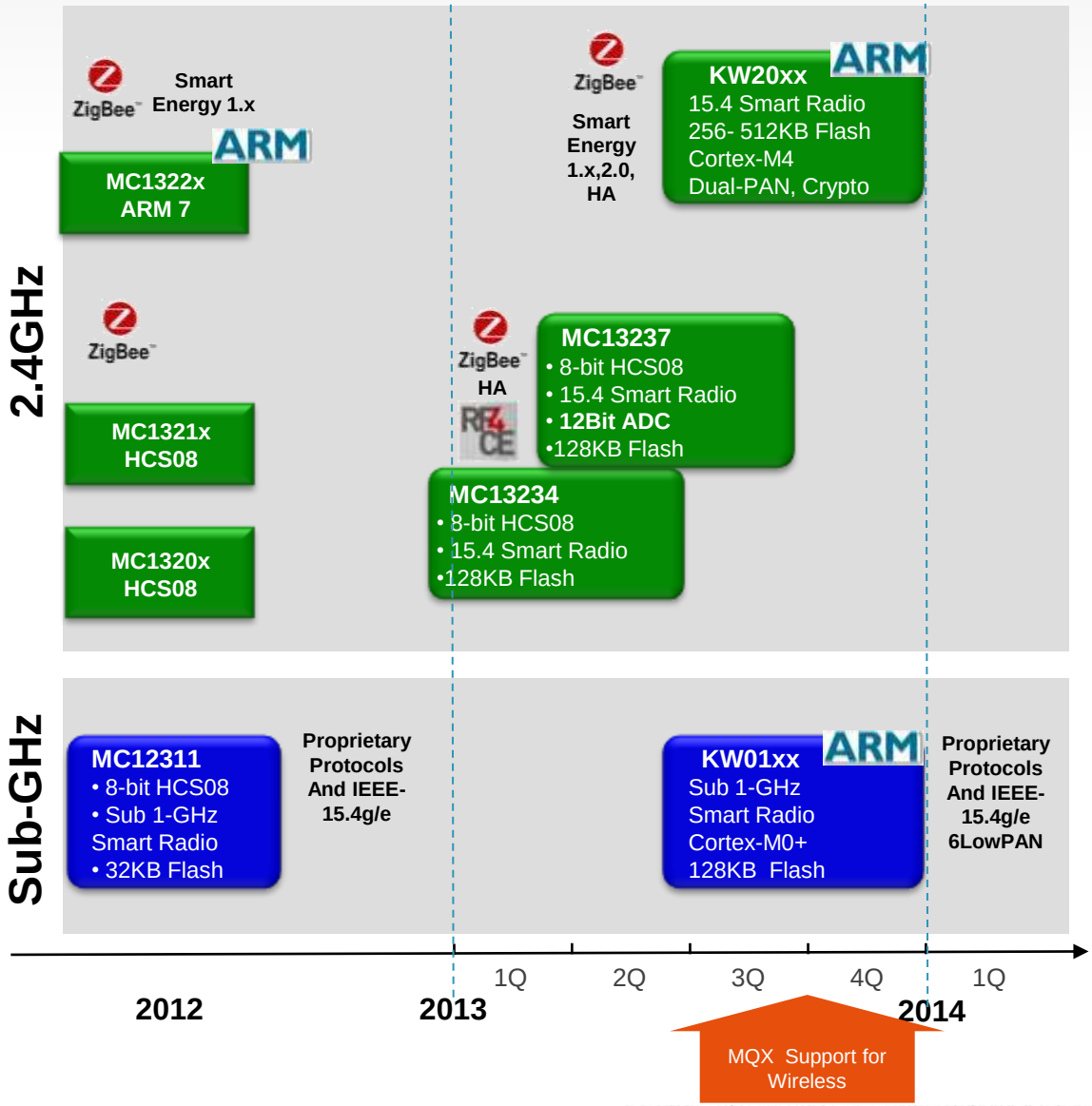
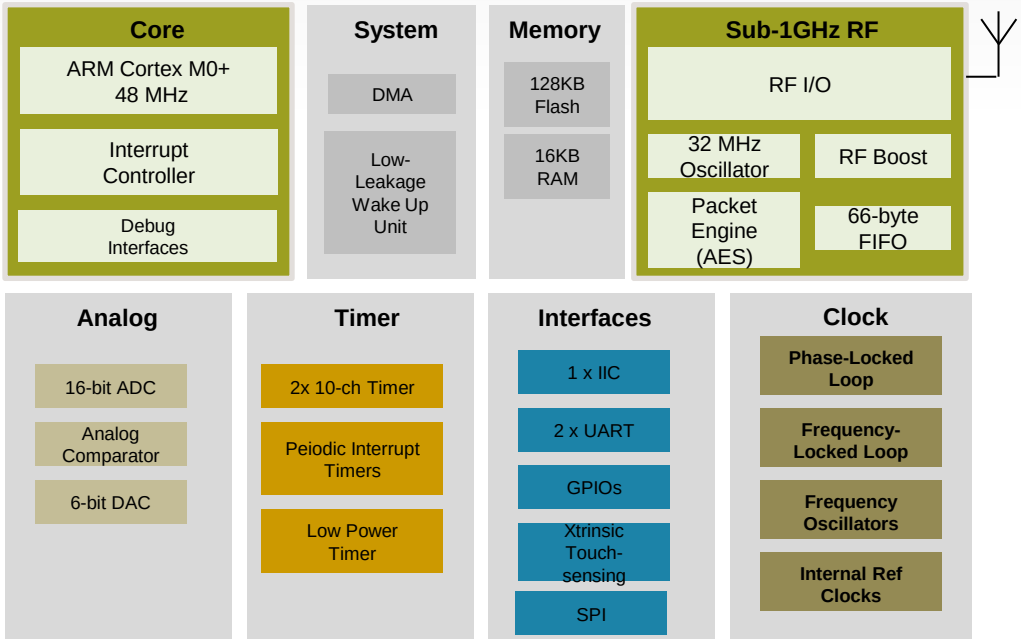
Freescale Wireless Portfolio



KW01 Wireless Kinetis Overview

- Microcontroller Features
  - 32-bit ARM Cortex M0+ 48MHz Core
  - Ultra Low Power
    - 30% power reduction from Cortex-M0
    - 56% increased energy efficiency from Cortex-M0
- 128KB Flash and 16KB SRAM
- Radio Transceiver Features
  - Supports 290-340MHz, 424-510MHz, and 862-1020MHz frequency bands
  - FSK, GFSK, MSK, GMSK and OOK modulations up to 600kbps
  - Up to -120dBm sensitivity @ 1.2kbps
  - -18 to +17dBm output in step of 1dBm
- Very low power suitable for battery operated devices
  - Ultra Low power stand-by modes
    - 1.7µA / 4.3µs wake-up time
  - 16 mA Rx current
  - 20 mA Tx current at 0 dBm
- Rich set of peripherals
  - 16-bit ADC, TSI, I2C, SPI, UART, Timers



Device	Flash / Flex	RAM	Package
MKW01Z128CHN	128 KB	16 KB	8x8 56-pin LGA
Features	**Description**		
Software and Protocol Stacks	Radio Utility 802.15.4g/e, SMAC		

Kinetis MKW20 Wireless MCU

CPU

- 50 MHz Cortex M4 CPU core
- Up to 512KB Flash, 64KB SRAM, 32KB Flex Mem, 4KB EEPROM
- Typical current consume: 250 uA/Mhz run, 1.7uA RTC standby

Radio Transceiver, 2.4GHz

- IEEE-802.15.4 compliant
- -100 Rx sensitivity and +10dBm Tx output power
- Peak typical current consume: 15mA Tx and 16.5mA Rx
- Dual Personal Area Network (PAN) support in hardware
  - Run two RF networks simultaneously
- Antenna diversity with automatic antenna selection

Security

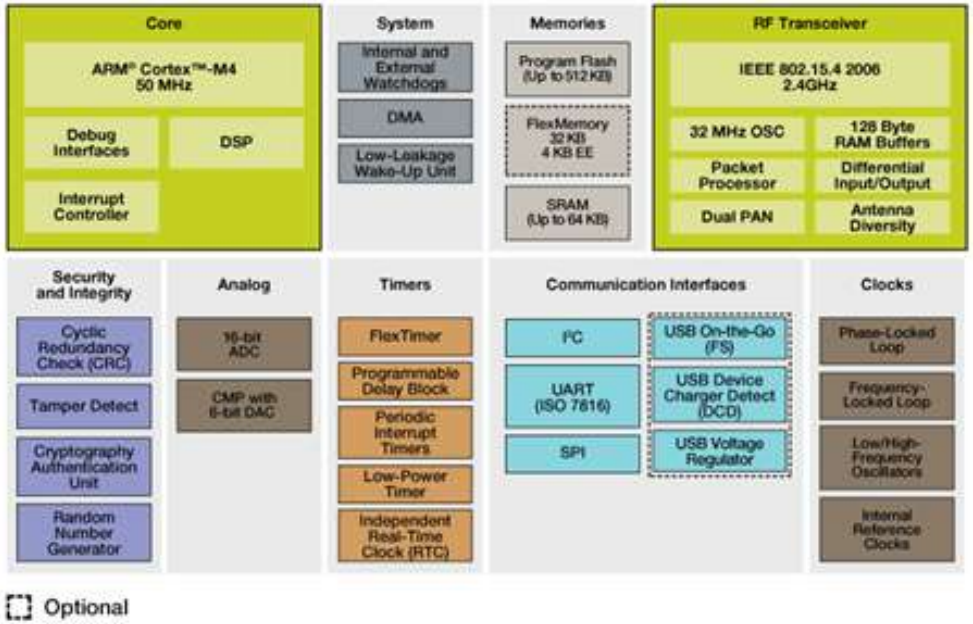
- Active and passive tamper detection with RTC timestamp
- Crypto engine: DES, 3DES, AES 128-256, SHA-1, SHA-256, MD5, RNG

Software

- 812.15.4 2006 MAC
- ZigBeePro, ZigBee IP
- Smart Energy 1.x & 2.0, HA 1.x, BA 1.x

System

- UART, SPI, I2C, optional USB 2.0 FS/LS H/D/OTG
- 16-bit ADC
- Operating range: 1.7V to 3.6V, -40C to +105C



Device	Flash	RAM	Feature	Package
MKW21D256VHA5	256 KB	32 KB	No USB	8x8 56-pin LGA
MKW22D512VHA5	512 KB	64 KB	USB	8x8 56-pin LGA
MKW24D512VHA5	512 KB	64 KB	USB and Smart Energy 2.0	8x8 56-pin LGA

Tools and Collateral to help you select the right Kinetis MCUs

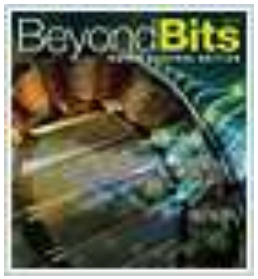
Online Selector Guide

Freescale Solutions Advisor @ freescale.com/solutionadvisor

Kinetis Find and Price Tool

Community site:
https://community.freescale.com/community/kinetis

Motor Control Brochure



Freescale Beyond Bits Motor Control Edition @ freescale.com/beyondbits

Short Printed Selector Guide

Kinetis Product Summaries @ freescale.com/kinetis

Freescale ARM Solutions

Featuring Kinetis, i.MX & Vybrid @ freescale.com/arm

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New MCU Solution Advisor: Interactive Product Selector Guide

- **Helps identify best MCU** choice by applying dynamic filters based on:
  - –Operating characteristics
  - –Packaging options
  - –Memory configuration
  - –Peripheral hardware library

- **Web-based application** featuring an interactive MCU product selector for Kinetis K, L series MCUs as well as 8-bit and Freescale DSC.

Now available:

Motor Control Wizard
Check pin-muxing
Interactive Tower System page

www.freescale.com/solutionadvisor

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