EVB72036

868/915MHz FSK/ASK Transmitter Evaluation Board Description

Features

- Fully integrated PLL-stabilized VCO
- Frequency range from 850 MHz to 930 MHz
- Single-ended RF output
- FSK through crystal pulling allows modulation from DC to 40 kbit/s
- High FSK deviation possible for wideband data transmission
- ASK achieved by on/off keying of internal power amplifier up to 40 kbit/s
- Wide power supply range from 1.95 V to 5.5 V
- Very low standby current
- Microcontroller clock output
- On-chip low voltage detector
- High over-all frequency accuracy
- FSK deviation and center frequency independently adjustable
- Adjustable output power range from -11 dBm to +9.5 dBm
- Adjustable current consumption from 5.5 mA to 13.8 mA
- Conforms to EN 300 220 and similar standards

Ordering Information

Part No. (see paragraph 5)

EVB72036-868-FSK-C

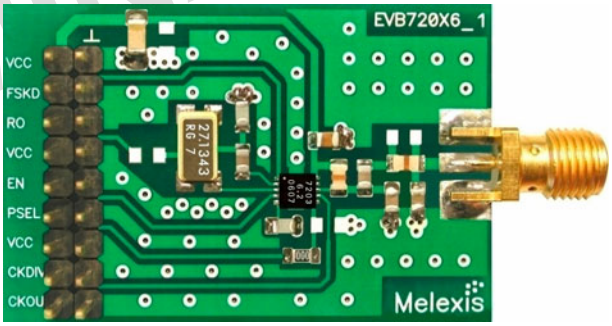
EVB72036-915-FSK-C

Note: EVB default population is FSK, ASK modification according to section 3.1.

Application Examples

- General digital data transmission
- Tire Pressure Monitoring Systems (TPMS)
- Remote Keyless Entry (RKE)
- Wireless access control
- Alarm and security systems
- Garage door openers
- Remote Controls
- Home and building automation
- Low-power telemetry systems

Evaluation Board Example



General Description

The TH72036 evaluation board is designed to demonstrate the performance of the transmitter IC for conductive measurements. The power amplifier is matched to 50 Ohms by means of a π-matching network to operate at a resonant frequency of 868 and 915 MHz.

The EVB72036 also features a clock output applicable to drive a microcontroller. The clock frequency can be selected by an external logic signal.

Document Content

1 Theory of Operation

1.1 General

As depicted in Fig.1, the TH72036 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-32 divider (div32), a phase-frequency detector (PFD) and a charge pump (CP). An internal loop filter determines the dynamic behavior of the PLL and suppresses reference spurious signals. A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. The VCO's output signal feeds the power amplifier (PA). The RF signal power P_{out} can be adjusted in four steps from P_{out} = –11 dBm to +9.5 dBm, either by changing the value of resistor RPS or by varying the voltage V_{PS} at pin PSEL. The open-collector output (OUT) can be used either to directly drive a loop antenna or to be matched to a 50Ohm load. Bandgap biasing ensures stable operation of the IC at a power supply range of 1.95 V to 5.5 V.

1.2 Block Diagram

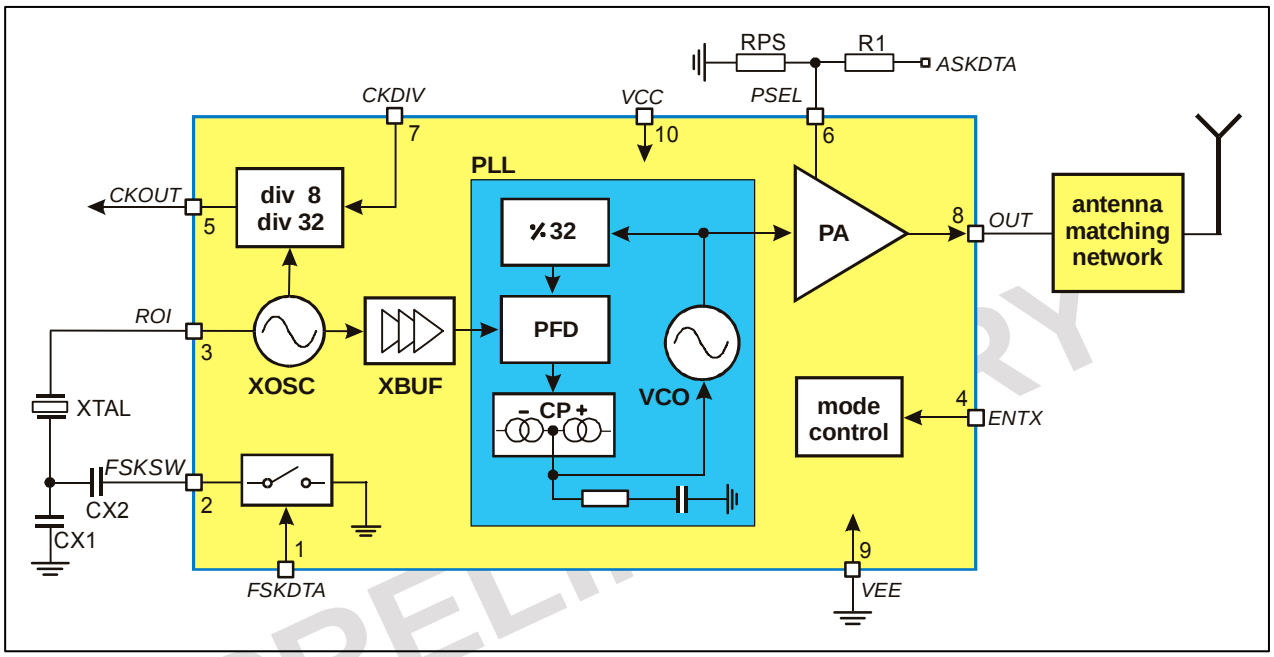


Fig. 1: Block diagram with external components

2 Functional Description

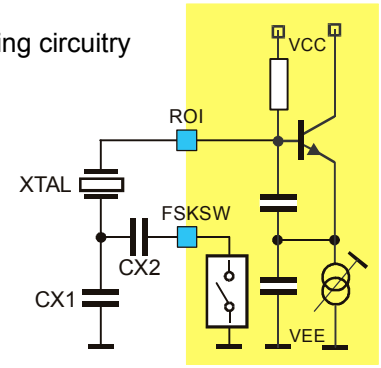
2.1 Crystal Oscillator

A Colpitts crystal oscillator with integrated functional capacitors is used as the reference oscillator for the PLL synthesizer. The equivalent input capacitance CRO offered by the crystal oscillator input pin ROI is about 18pF. The crystal oscillator is provided with an amplitude control loop in order to have a very stable frequency over the specified supply voltage and temperature range in combination with a short start-up time.

2.2 FSK Modulation

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at the pin FSKDTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and the center frequency f_c to be adjusted independently. At FSKDTA = 0, CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at FSKDTA = 1, CX2 is deactivated and the XOSC is set to its high frequency f_{max}.
An external reference signal can be directly AC-coupled to the reference oscillator input pin ROI. Then the transmitter is used without a crystal. Now the reference signal sets the carrier frequency and may also contain the FSK (or FM) modulation.

Fig. 2: Crystal pulling circuitry



FSKDTA	Description
0	$f_{min} = f_c - \Delta f$ (FSK switch is closed)
1	$f_{max} = f_c + \Delta f$ (FSK switch is open)

2.3 Crystal Pulling

A crystal is tuned by the manufacturer to the required oscillation frequency f_0 at a given load capacitance CL and within the specified calibration tolerance. The only way to pull the oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.
Figure 3 shows the oscillation frequency of a crystal as a function of the effective load capacitance. This capacitance changes in accordance with the logic level of FSKDTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.
It can also be seen that the pulling sensitivity increases with the reduction of CL. Therefore, applications with a high frequency deviation require a low load capacitance. For narrow band FSK applications, a higher load capacitance could be chosen in order to reduce the frequency drift caused by the tolerances of the chip and the external pulling capacitors.

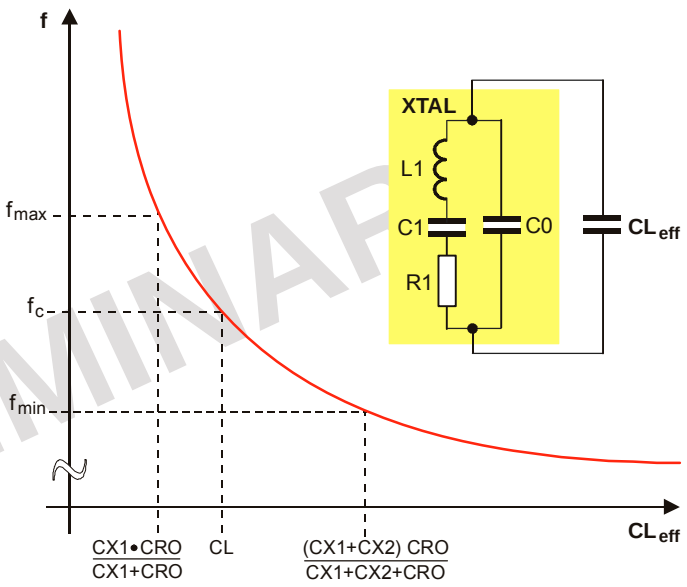


Fig. 3: Crystal pulling characteristic

For ASK applications CX2 can be omitted. Then CX1 has to be adjusted for center frequency.

2.4 ASK Modulation

The TH72036 can be ASK-modulated by applying data directly at pin PSEL. This turns the PA on and off which leads to an ASK signal at the output.

2.5 Output Power Selection

The transmitter is provided with an output power selection feature. There are four predefined output power steps and one off-step accessible via the power selection pin PSEL. A digital power step adjustment was chosen because of its high accuracy and stability. The number of steps and the step sizes as well as the corresponding power levels are selected to cover a wide spectrum of different applications.

The implementation of the output power control logic is shown in figure 4. There are two matched current sources with an amount of about 8 µA. One current source is directly applied to the PSEL pin. The other current source is used for the generation of reference voltages with a resistor ladder. These reference voltages are defining the thresholds between the power steps. The four comparators deliver thermometer-coded control signals depending on the voltage level at the pin PSEL. In order to have a certain amount of ripple tolerance in a noisy environment the comparators are provided with a little hysteresis of about 20 mV. With these control signals, weighted current sources of the power amplifier are switched on or off to set the desired output power level (Digitally Controlled Current Source). The LOCK, ASK signal and the output of the low voltage detector are gating this current source.

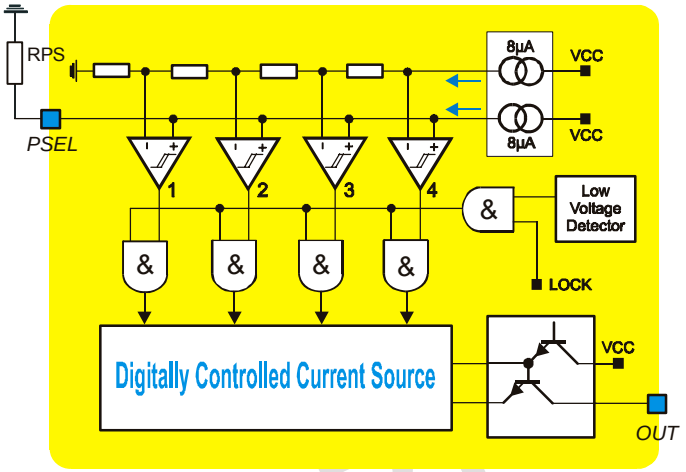


Fig. 4: Block diagram of output power control circuitry

There are two ways to select the desired output power step. First by applying a DC voltage at the pin PSEL, then this voltage directly selects the desired output power step. This kind of power selection can be used if the transmission power must be changed during operation. For a fixed-power application a resistor can be used which is connected from the PSEL pin to ground. The voltage drop across this resistor selects the desired output power level. For fixed-power applications at the highest power step this resistor can be omitted. The pin PSEL is in a high impedance state during the “TX standby” mode.

2.6 Lock Detection

The lock detection circuitry turns on the power amplifier only after PLL lock. This prevents from unwanted emission of the transmitter if the PLL is unlocked.

2.7 Low Voltage Detection

The supply voltage is sensed by a low voltage detect circuitry. The power amplifier is turned off if the supply voltage drops below a value of about 1.85 V. This is done in order to prevent unwanted emission of the transmitter if the supply voltage is too low.

2.8 Mode Control Logic

The mode control logic allows two different modes of operation as listed in the following table. The mode control pin EN is pulled-down internally. This guarantees that the whole circuit is shut down if this pin is left floating.

EN	Mode	Description
0	TX standby	TX disabled
1	TX active CKOUT active	TX / CKOUT enabled

2.9 Clock Output

The clock output CKOUT is CMOS-compatible and can be used to drive a microcontroller. The frequency of the clock can be changed by the clock divider control signal CKDIV, that can be selected according to the following table. A capacitor at pin CKOUT can be used to control the clock voltage swing and the spurious emission.

CKDIV	Clock divider ratio	Clock frequency / f_c=433.92 MHz
0	4	3.39 MHz
1	16	848 kHz

2.10 Timing Diagrams

After enabling the transmitter by the EN signal, the power amplifier remains inactive for the time t_{on}, the transmitter start-up time. The crystal oscillator starts oscillation and the PLL locks to the desired output frequency within the time duration t_{on}. After successful PLL lock, the LOCK signal turns on the power amplifier, and then the RF carrier can be FSK or ASK modulated.

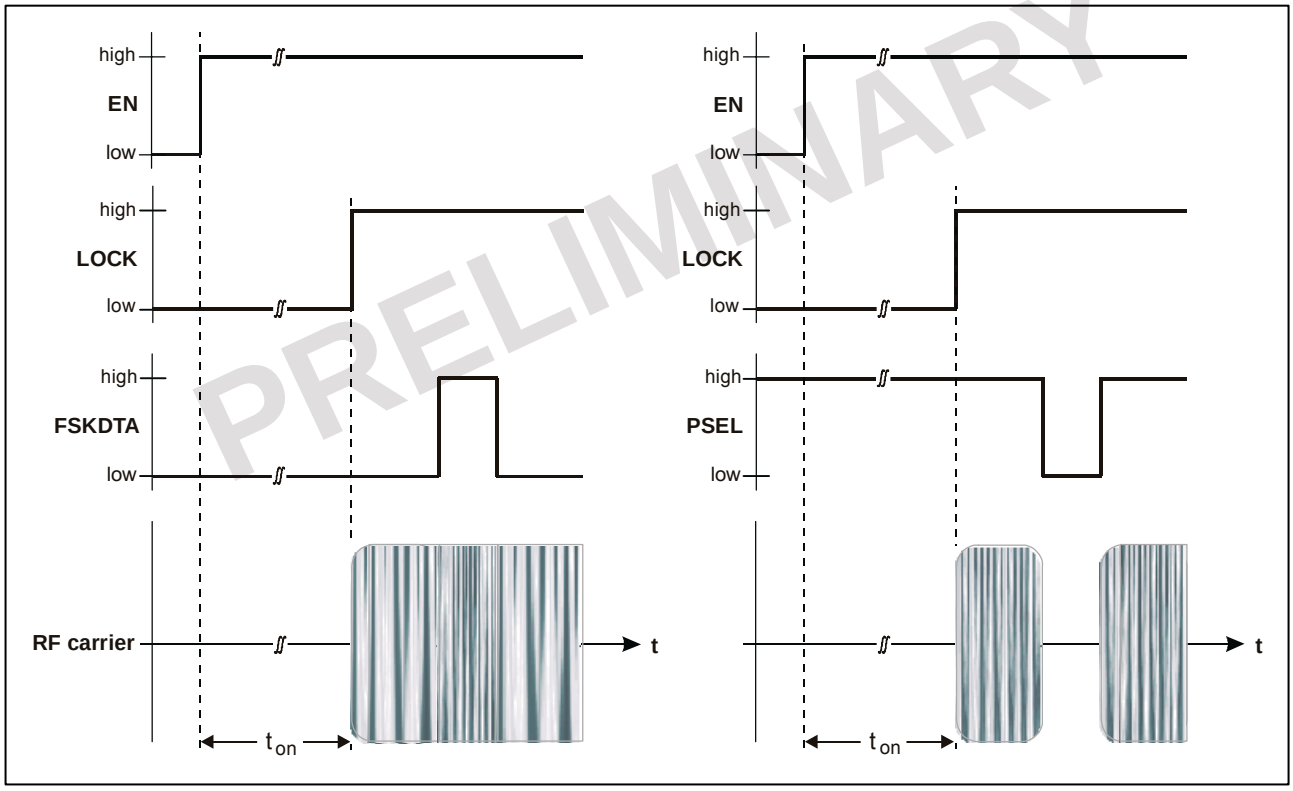


Fig. 5: Timing diagrams for FSK and ASK modulation

For more detailed information, please refer to the latest TH72036 data sheet revision.

3 50Ω Connector Board Circuit Diagram

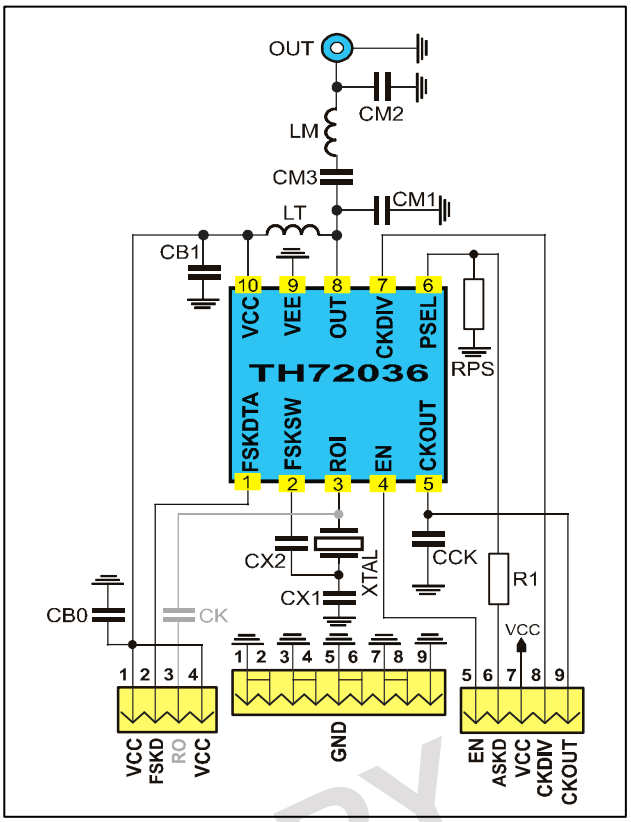


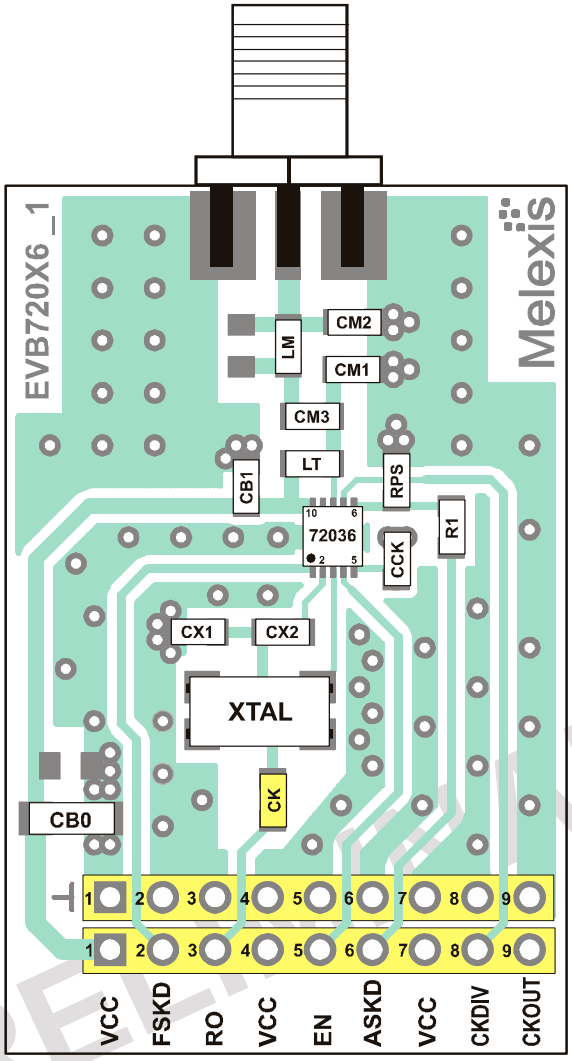
Fig. 6: Circuit diagram with 50 Ω matching network

3.1 Board Component Values

Part	Size	Value @ 868.3 MHz	Value @ 915 MHz	Toler-ance	Description
CM1	0805	1.8 pF	2.2 pF	±5%	impedance matching capacitor
CM2	0805	5.6 pF	5.6 pF	±5%	impedance matching capacitor
CM3	0805	68 pF	68 pF	±5%	impedance matching capacitor r
LM	0805	12 nH	10 nH	±5%	impedance matching inductor
LT	0805	15 nH	10 nH	±5%	output tank inductor
$CX1_{FSK}$	0805	22 pF	22 pF	±5%	XOSC FSK capacitor (Δf = ±20 kHz), note 1
$CX1_{ASK}$	0805	27 pF	27 pF	±5%	XOSC ASK capacitor, trimmed to f_C, note 1
CX2	0805	12pF	12 pF	±5%	XOSC capacitor (Δf = ±20 kHz), note 1, only for FSK
CCK	0805	15 pF/ 180 pF		±5%	capacitor to control clock voltage swing (CKDIV 0 / 1)
RPS	0805	NIP		±5%	power-select resistor, see data sheet section 4.6
R1	0805	0 Ω		±5%	ASK jumper (for ASK only), see data sheet sect. 4.7
CB0	1206	220 nF		±20%	de-coupling capacitor
CB1	0805	330 pF		±10%	de-coupling capacitor
XTAL	SMD 6x3.5	27.13438 MHz	28.59375 MHz		fundamental mode crystal, C_L = 12 pF, $C_{0,\,max}$ = 7 pF, R_1 = 40 Ω
		±30ppm cali., ±30ppm temp			
CK	0805	1 nF		±10%	ROI coupling capacitor, only required for external reference frequency input

Note 1: depends on crystal parameters, other Δf values can be selected with other CX1, CX2 values
NIP – not in place, may be used optionally

3.2 50Ω Connector Board PCB Top View



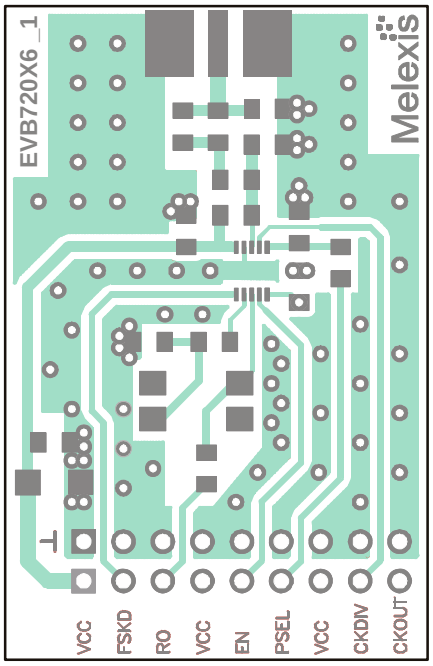
Board size is 27 mm x 42 mm

3.3 Board Connection

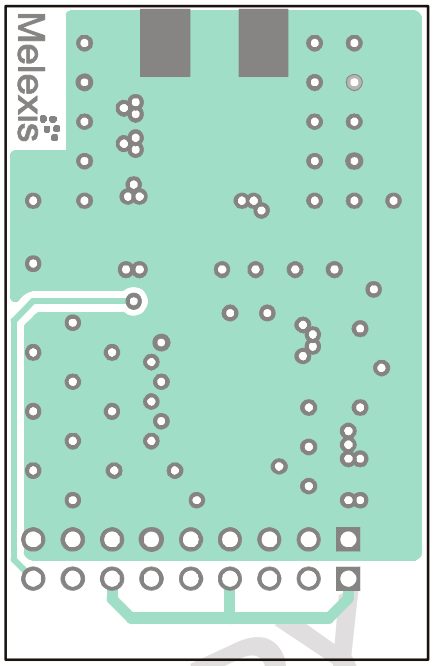
VCC	Power supply (1.95 V to 5.5 V)	**CKDIV**	Clock divider input, (CMOS, see sect. 2.9)
FSKD	Input for FSK data (CMOS, see section 2.2)	**CKOUT**	Clock output, (CMOS, see section 2.9)
ASKD	Input for ASK data (CMOS, see section 2.4)	**RO**	External reference frequency input
EN	Mode control pin (see par. 2.8)	⊥	Several ground pins

4 Evaluation Board Layout

Board layout data in Gerber format are available, board size is 27mm x 42mm x 1mm FR4.



PCB top view



PCB bottom view

5 Board Variants

Type	Frequency/MHz	Modulation	Board Execution
EVB72005	**–315**	**–FSK**	**–A** antenna version
	–433	**–ASK** according to section 3.1	**–C** connector version
	–868	**–FM**	
	–915		

Note: **available EVB setups**

6 Package Description

The device TH72016 is RoHS compliant.

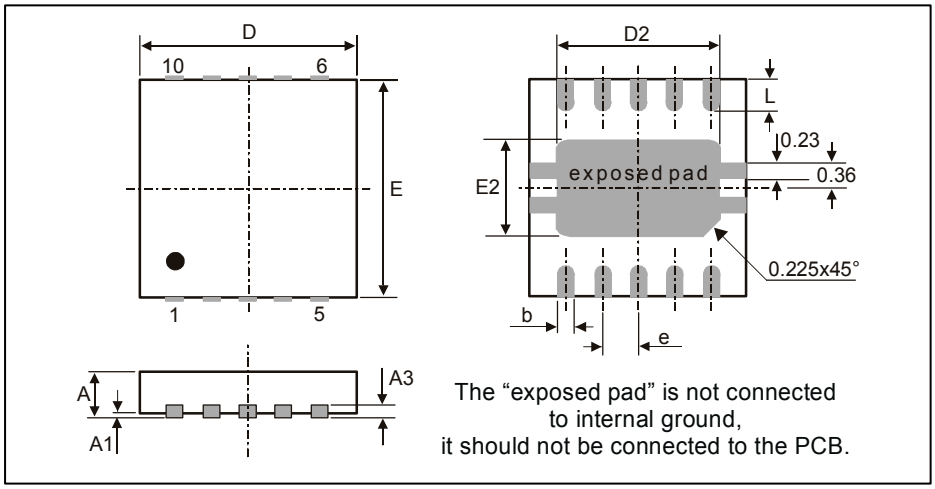


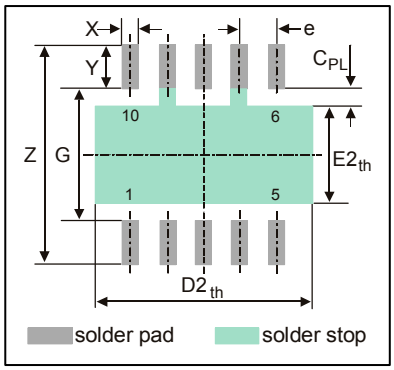
Fig. 7: 10L QFN 3x3 Dual

all Dimensions in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	2.85	2.85	2.23	1.49	0.80	0	0.20	0.3	0.50	0.18
max	3.15	3.15	2.48	1.74	1.00	0.05		0.5		0.30
all Dimensions in inch										
min	0.112	0.112	0.0878	0.051	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.124	0.124	0.0976	0.055	0.0393	0.002		0.0197		0.0118

6.1 Soldering Information

- The device TH72036 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

6.2 Recommended PCB Footprints



all Dimensions in mm								
	Z	**G**	**D2$_{th}$**	**E2$_{th}$**	**X**	**Y**	**C$_{PL}$**	**e**
min	3.55	1.9	3.2	1.3	0.25	0.7	0.3	0.5
max	3.90	2.3	3.6	1.7	0.30	1.0	0.5	
all Dimensions in inch								
min	0.1398	0.0748	0.1260	0.0512	0.0098	0.0276	0.0591	0.0197
max	0.1535	0.0906	0.1417	0.0669	0.0118	0.0394	0.0197	

Fig. 8: PCB land pattern style

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Europe, Africa:	Americas:	Asia:
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