

Vishay Semiconductors

ADD-A-PAK Generation VII Power Modules Thyristor/Thyristor, 105 A



| PRODUCT SUMMARY | | | | | | |
|--------------------|-------------------------------|--|--|--|--|--|
| I _{T(AV)} | 105 A | | | | | |
| Туре | Modules - Thyristor, Standard | | | | | |

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- High voltage
- Industrial standard package
- UL approved file E78996
- · Low thermal resistance
- · Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- · High surge capability
- · Easy mounting on heatsink

ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

| MAJOR RATINGS AND CHARACTERISTICS | | | | | | |
|-----------------------------------|-----------------|-------------|-------------------|--|--|--|
| SYMBOL | CHARACTERISTICS | UNITS | | | | |
| I _{T(AV)} | 85 °C | 105 | | | | |
| I _{T(RMS)} | | 165 | А | | | |
| I _{TSM} | 50 Hz | 2000 | A | | | |
| | 60 Hz | 2094 | | | | |
| l ² t | 50 Hz | 20 | kA ² s | | | |
| 1-1 | 60 Hz | 18.26 | KA-S | | | |
| I²√t | | 200 | kA²√s | | | |
| V _{RRM} | Range | 400 to 1600 | V | | | |
| T _{Stg} | | -40 to 130 | °C | | | |
| T _J | | -40 to 130 | °C | | | |

VS-VSKU105.., VS-VSKV105.. Series

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ELECTRICAL SPECIFICATIONS

| VOLTAGE RATINGS | | | | | | | | | |
|-----------------|-----------------|---|---|--|---|--|--|--|--|
| TYPE NUMBER | VOLTAGE CODE | V _{RRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V | V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V | V _{DRM} , MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V | I _{RRM,} I _{DRM} AT 130 °C mA | | | | |
| | 04 | 400 | 500 | 400 | | | | | |
| VS-VSK.105 | 08 | 800 | 900 | 800 | 15 | | | | |
| 12 | | 1200 | 1300 | 1200 | 13 | | | | |
| | 16 | 1600 | 1700 | 1600 | | | | | |

| PARAMETER | SYMBOL | 7 | EST CONDITION | TEST CONDITIONS | | |
|--|----------------------------------|--|--|---------------------------|-------|-------------------|
| Maximum average on-state current | I _{T(AV)} | 180° conduction T _C = 85 °C | 180° conduction, half sine wave, T _C = 85 °C | | 105 | A |
| Maximum continuous RMS on-state current | | DC | | | 165 | |
| Maximum continuous Rivis on-state current | I _{T(RMS)} | T _C | | | 78 | °C |
| | | t = 10 ms | No voltage | Sinusoidal | 2000 | |
| Maximum peak, one-cycle non-repetitive | ١. | t = 8.3 ms | reapplied | half wave, | 2094 | ۸ |
| on-state current | I _{TSM} | t = 10 ms | 100 % V _{RRM} | initial T _J = | 1682 | А |
| | | t = 8.3 ms | reapplied | T _J maximum | 1760 | |
| Maximum I ² t for fusing | | t = 10 ms No voltage | 20 | | | |
| | l ² t | t = 8.3 ms | reapplied | Initial T _{.I} = | 18.26 | kA ² s |
| | | t = 10 ms | 100 % V _{RRM} | T _J maximum | 14.14 | |
| | | t = 8.3 ms | reapplied | | 12.91 | |
| Maximum $I^2\sqrt{t}$ for fusing | I ² √t ⁽¹⁾ | $t = 0.1 \text{ ms to } 1000 \text{ ms}$ $T_J = T_J \text{ maximum}$ | t = 0.1 ms to 10 ms, no voltage reapplied T = T maximum | | | kA²√s |
| | (0) | Low level (3) | | | 0.98 | |
| Maximum value of threshold voltage | V _{T(TO)} (2) | High level (4) | $T_J = T_J \text{ maxin}$ | num | 1.12 | V |
| Maximum value of on-state | (0) | Low level (3) | | | 2.7 | |
| slope resistance | r _t (2) | High level (4) | $T_J = T_J$ maximum | | 2.34 | mΩ |
| Maximum on-state voltage drop | V _{TM} | $I_{TM} = \pi \times I_{T(AV)}$ $T_J = 25 ^{\circ}C$ | | 1.8 | V | |
| Maximum non-repetitive rate of rise of turned on current | dl/dt | $T_J = 25$ °C, from 0.67 V_{DRM} , $I_{TM} = \pi \times I_{T(AV)}$, $I_g = 500$ mA, $t_r < 0.5$ μ s, $t_p > 6$ μ s | | 150 | A/µs | |
| Maximum holding current | I _H | T _J = 25 °C, anode supply = 6 V, resistive load, gate open circuit | | | 250 | mA |
| Maximum latching current | ΙL | T _J = 25 °C, and | ode supply = 6 \ | /, resistive load | 400 | |

Notes

⁽¹⁾ I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$

⁽²⁾ Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$

^{(3) 16.7 %} x π x I_{AV} < I < π x I_{AV}

⁽⁴⁾ $I > \pi \times I_{AV}$

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| TRIGGERING | | | | | |
|--|--------------------|---|---|--------|-------|
| PARAMETER | SYMBOL | TEST CO | NDITIONS | VALUES | UNITS |
| Maximum peak gate power | P _{GM} | | | 12 | W |
| Maximum average gate power | P _{G(AV)} | | | 3.0 | VV |
| Maximum peak gate current | I _{GM} | | | 3.0 | Α |
| Maximum peak negative gate voltage | - V _{GM} | | | 10 | . V |
| | | T _J = - 40 °C | Anode supply = 6 V resistive load | 4.0 | |
| Maximum gate voltage required to trigger | V_{GT} | T _J = 25 °C | | 2.5 | |
| | | T _J = 125 °C | | 1.7 | |
| | | T _J = - 40 °C | Anode supply = 6 V | 270 | |
| Maximum gate current required to trigger | I _{GT} | T _J = 25 °C | | 150 | mA |
| | | T _J = 125 °C | - resistive load | 80 | |
| Maximum gate voltage that will not trigger | V_{GD} | T _J = 125 °C, rated V _{DRM} applied | | 0.25 | V |
| Maximum gate current that will not trigger | I _{GD} | $T_J = 125 ^{\circ}\text{C}$, rated V_{DR} | T _J = 125 °C, rated V _{DRM} applied | | mA |

| BLOCKING | | | | | | | | |
|---|---------------------------------------|--|----------------------------|-------|--|--|--|--|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS | | | | |
| Maximum peak reverse and off-state leakage current at V _{RRM} , V _{DRM} | I _{RRM,} I _{DRM} | T _J = 130 °C, gate open circuit | 20 | mA | | | | |
| Maximum RMS insulation voltage | V _{INS} | 50 Hz | 3000 (1 min) 3600 (1 s) | V | | | | |
| Maximum critical rate of rise of off-state voltage | dV/dt | T_J = 130 °C, linear to 0.67 V_{DRM} | 1000 | V/µs | | | | |

| THERMAL AND MECHANICAL SPECIFICATIONS | | | | | |
|---|-------------|-----------------------------------|---|------------|--------------|
| PARAMETER | | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| Junction operating and storage temperature range | | T _J , T _{Stg} | | -40 to 130 | °C |
| Maximum internal thermal resistance, junction to case per leg | | R _{thJC} | DC operation | 0.22 | °C/W |
| Typical thermal resistance, case to heatsink per module | | R _{thCS} | Mounting surface flat, smooth and greased | 0.1 | C/VV |
| Mounting torque ± 10 % | to heatsink | | A mounting compound is recommended and the torque should be rechecked after a period of | 4 | Nm |
| busbar | | | 3 hours to allow for the spread of the compound. | 3 | IVIII |
| Approximate weight | | | | 75 | g |
| Approximate weight | | | | 2.7 | oz. |
| Case style | | | JEDEC® | AAP GEN VI | I (TO-240AA) |

| △R CONDUCTION PER JUNCTION | | | | | | | | | | | |
|----------------------------|------|---------------------------|-------|-------|-------|-------|---------|-----------|------------|-------|-------|
| DEVICES | 5 | SINE HALF WAVE CONDUCTION | | | | | CTANGUL | AR WAVE C | CONDUCTION | NC | UNITS |
| DEVICES | 180° | 120° | 90° | 60° | 30° | 180° | 120° | 90° | 60° | 30° | UNITS |
| VSK.105 | 0.04 | 0.048 | 0.063 | 0.085 | 0.125 | 0.033 | 0.052 | 0.067 | 0.088 | 0.127 | °C/W |

Note

Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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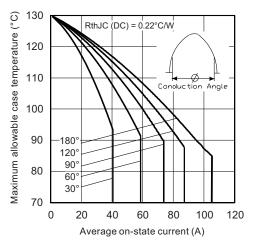


Fig. 1 - Current Ratings Characteristics

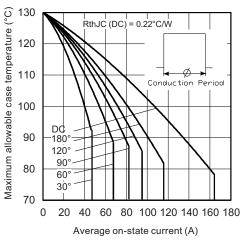


Fig. 2 - Current Ratings Characteristics

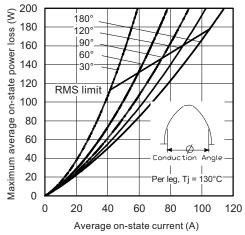


Fig. 3 - On-State Power Loss Characteristics

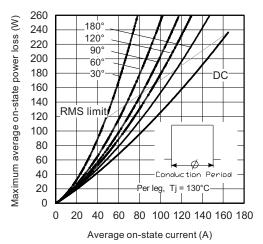
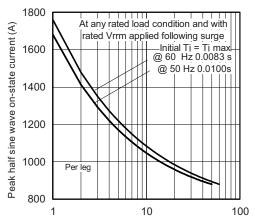


Fig. 4 - On-State Power Loss Characteristics



Number of equal amplitude half cycle current pulses (N)

Fig. 5 - Maximum Non-Repetitive Surge Current

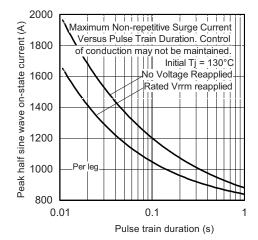


Fig. 6 - Maximum Non-Repetitive Surge Current

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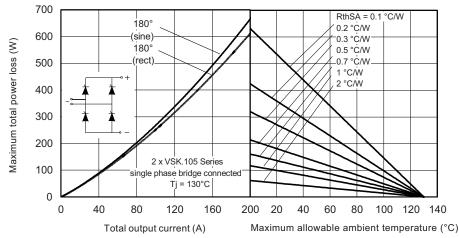


Fig. 7 - On-State Power Loss Characteristics

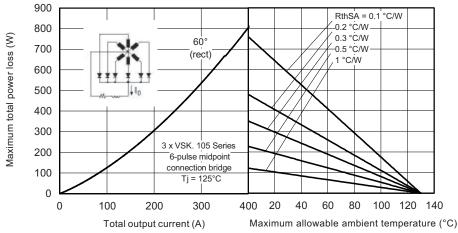


Fig. 8 - On-State Power Loss Characteristics

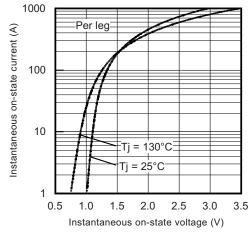


Fig. 9 - On-State Voltage Characteristics

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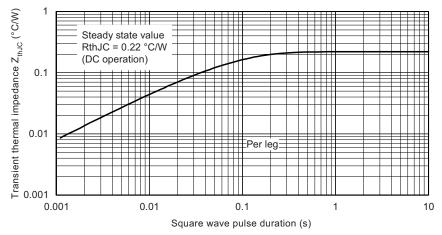


Fig. 10 - Thermal Impedance Z_{thJC} Characteristics

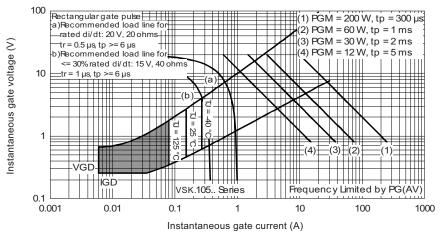
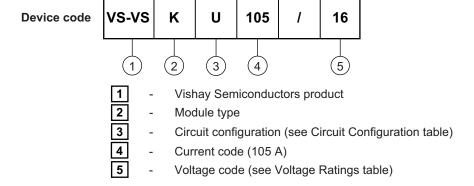


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE



Note

• To order the optional hardware go to www.vishay.com/doc?95172

VS-VSKU105.., VS-VSKV105.. Series

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| CIRCUIT CONFIGURATION | CIRCUIT CONFIGURATION | | | | | | |
|--------------------------|-------------------------------|--|--|--|--|--|--|
| CIRCUIT DESCRIPTION | CIRCUIT CONFIGURATION CODE | CIRCUIT DRAWING | | | | | |
| Two SCRs common cathodes | U | VSKU (1) 1 2 (2) (3) (3) (3) (4) (5) (7) (6) | | | | | |
| Two SCRs common anodes | V | VSKV (1) (2) (3) (3) (3) (3) (4) (5) (7) (6) | | | | | |

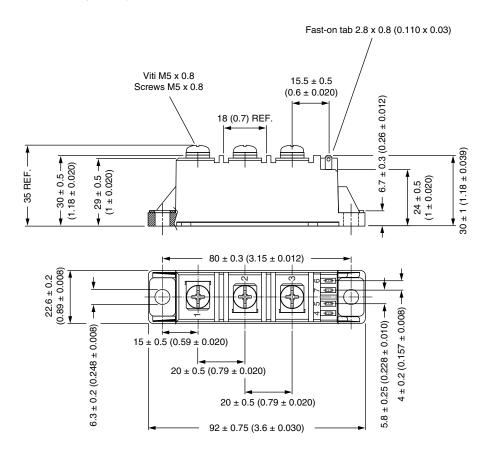
| LINKS TO RELATED DOCUMENTS | | | | |
|----------------------------|--------------------------|--|--|--|
| Dimensions | www.vishay.com/doc?95368 | | | |



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ADD-A-PAK Generation VII - Thyristor

DIMENSIONS in millimeters (inches)





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