ALPHA & OMEGA SEMICONDUCTOR

# AO4454

## 100V N-Channel MOSFET
## SDMOS™

## General Description

The AO4454 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge.The result is outstanding efficiency with controlled switching behaviar. This universal technology is well suited for PWM, load switching and general purpose applications.

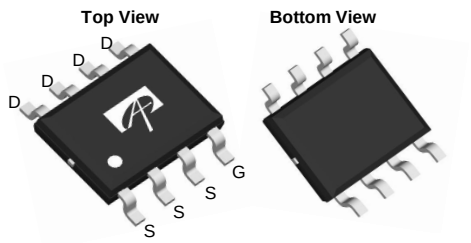
## Product Summary

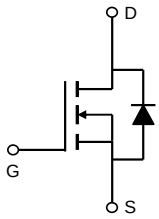
| | |
|---|---|
| $V_{DS}$ | 100V |
| $I_D$ (at $V_{GS}$=10V) | 6.5A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | < 36mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 7V) | < 43mΩ |

100% UIS Tested
100% $R_g$ Tested

Green Product

SOIC-8




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±25 | V |
| Continuous Drain Current | $T_A$=25°C | $I_D$ | 6.5 | A |
| | $T_A$=70°C | | 5.3 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 46 | |
| Avalanche Current [C] | | $I_{AS}$, $I_{AR}$ | 28 | A |
| Avalanche energy L=0.1mH [C] | | $E_{AS}$, $E_{AR}$ | 39 | mJ |
| Power Dissipation [B] | $T_A$=25°C | $P_D$ | 3.1 | W |
| | $T_A$=70°C | | 2 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 31 | 40 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 59 | 75 | °C/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 16 | 24 | °C/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 100 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=100V, $V_{GS}$=0V | | | 10 | µA |
| | | $T_J$=55°C | | | 50 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±25V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 2.8 | 3.4 | 4 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 46 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=6.5A | | 30 | 36 | mΩ |
| | | $T_J$=125°C | | 56 | 67 | |
| | | $V_{GS}$=7V, $I_D$=6A | | 35.5 | 43 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=6.5A | | 20 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.68 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 4 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=50V, f=1MHz | 950 | 1180 | 1450 | pF |
| $C_{oss}$ | Output Capacitance | | 77 | 110 | 145 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 21 | 36 | 50 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.35 | 0.7 | 1.05 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=50V, $I_D$=6.5A | 15 | 19 | 23 | nC |
| $Q_{gs}$ | Gate Source Charge | | 5.5 | 7 | 8.5 | nC |
| $Q_{gd}$ | Gate Drain Charge | | 3.5 | 6.3 | 9 | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=50V, $R_L$=6.7Ω, $R_{GEN}$=3Ω | | 10 | | ns |
| $t_r$ | Turn-On Rise Time | | | 7.2 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 15 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 7 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=6.5A, dI/dt=500A/µs | 11 | 16 | 21 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=6.5A, dI/dt=500A/µs | 35 | 50 | 65 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

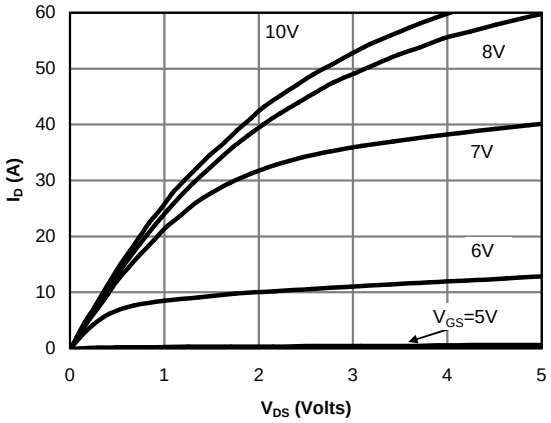



**Fig 1: On-Region Characteristics (Note E)**

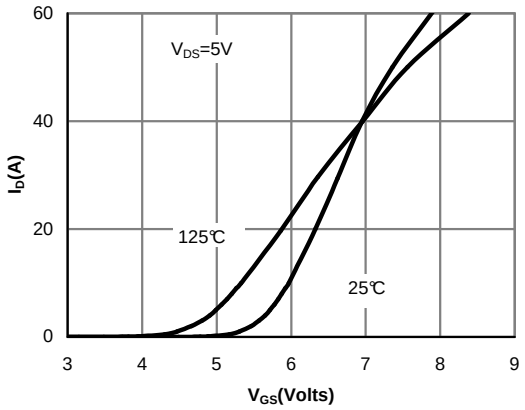



**Figure 2: Transfer Characteristics (Note E)**

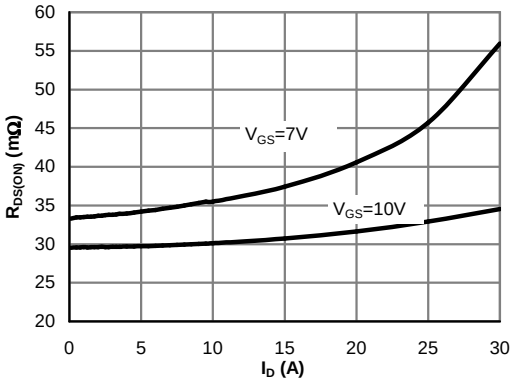



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

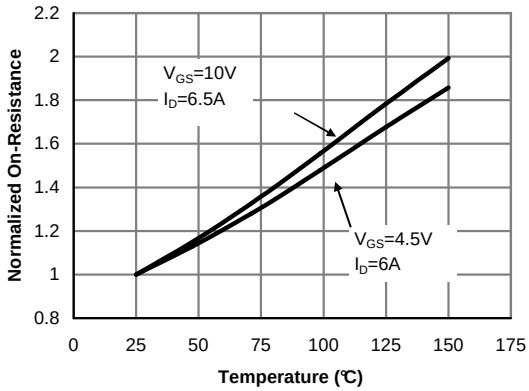



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

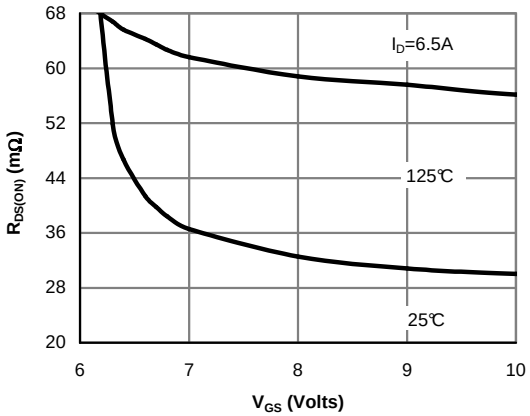



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

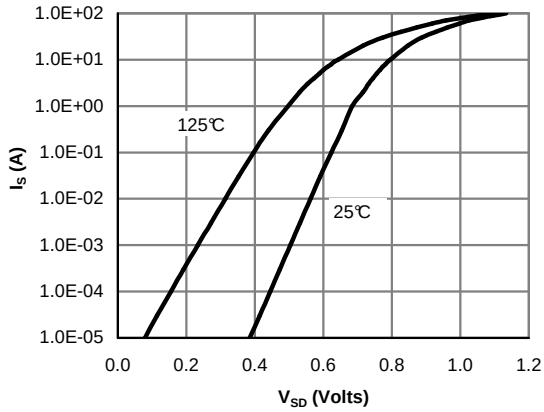



**Figure 6: Body-Diode Characteristics (Note E)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

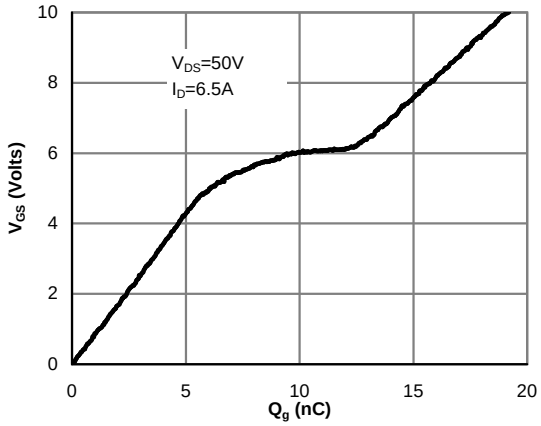



Figure 7: Gate-Charge Characteristics

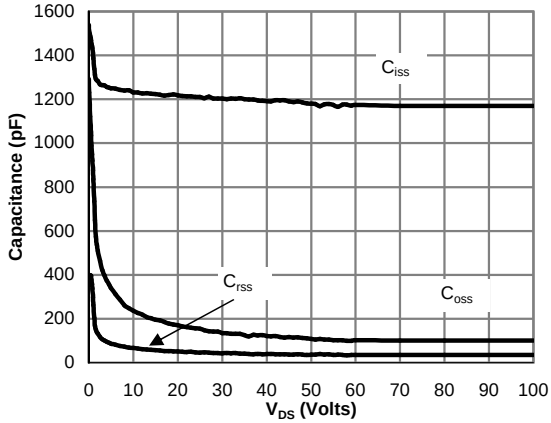



Figure 8: Capacitance Characteristics

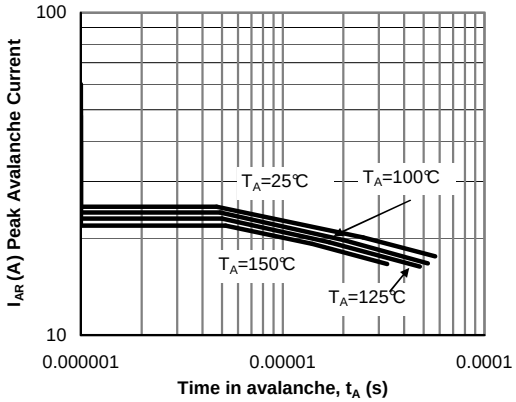



Figure 9: Single Pulse Avalanche capability (Note C)

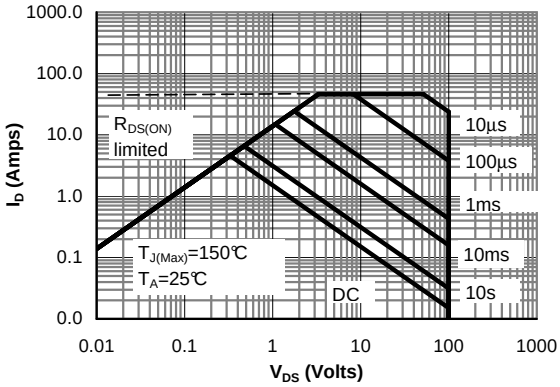



Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

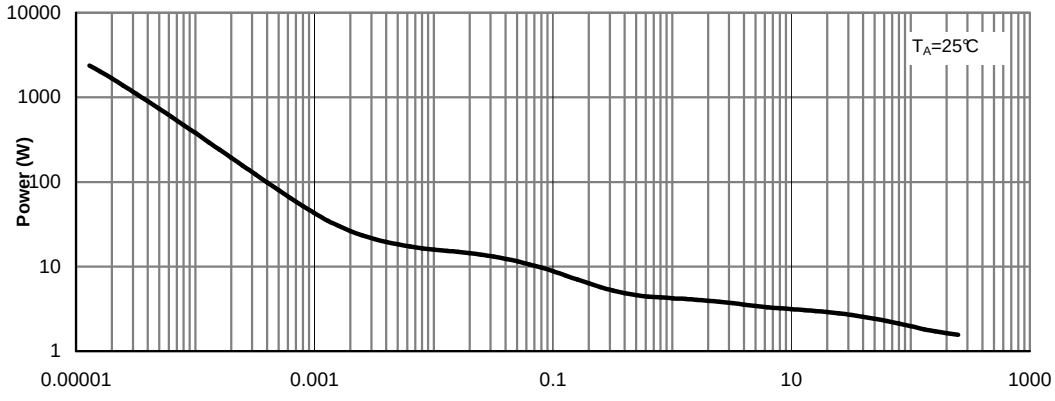



Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

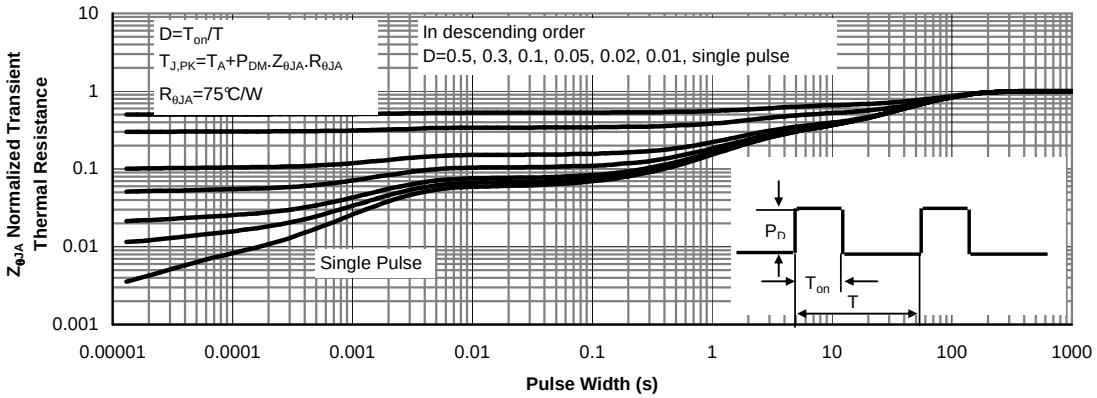



**Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)**

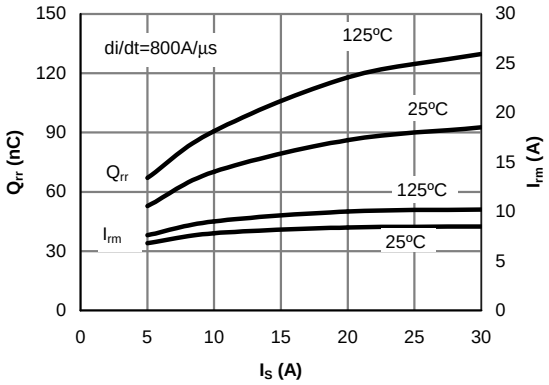



**Figure 13: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**

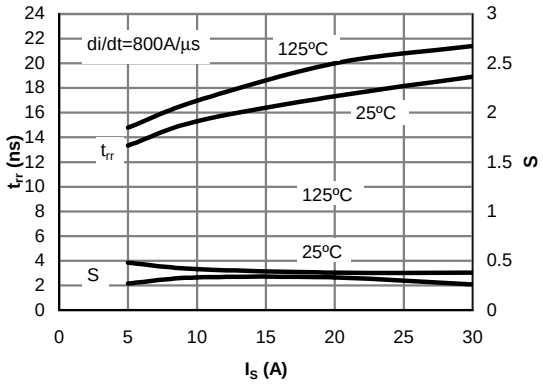



**Figure 14: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

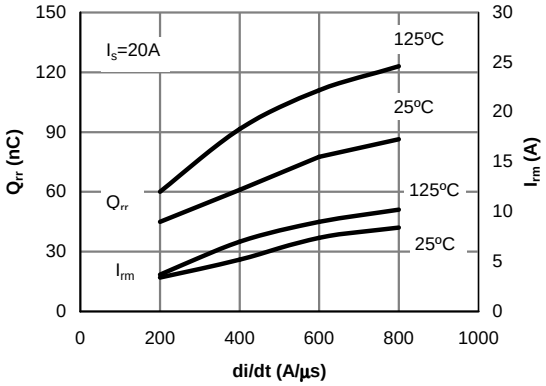



**Figure 15: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

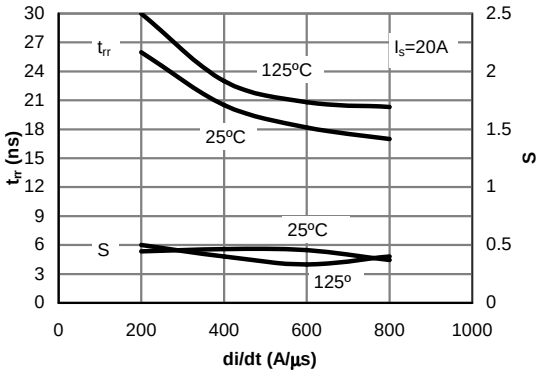
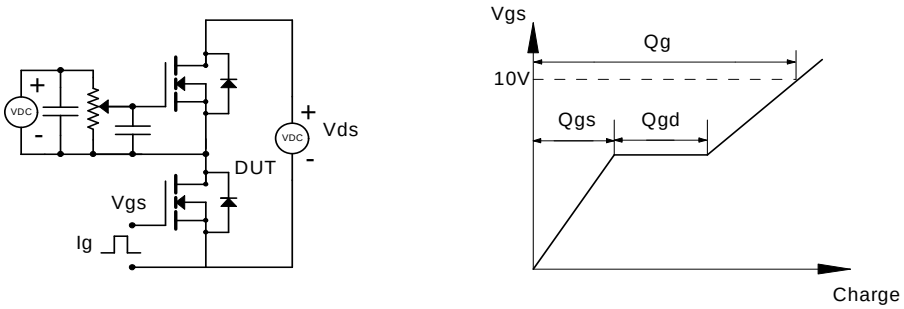
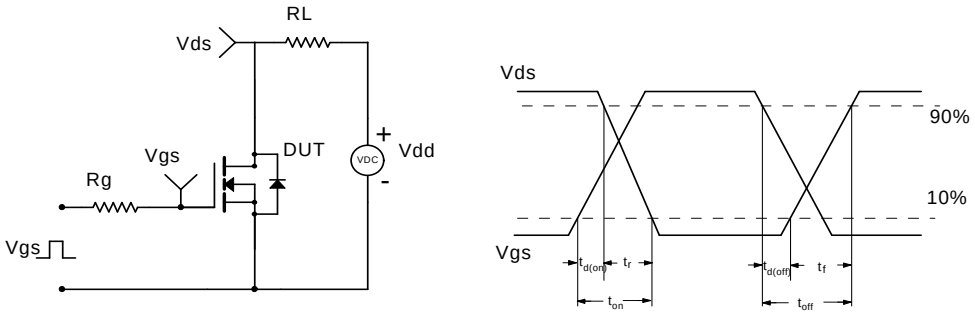



**Figure 16: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

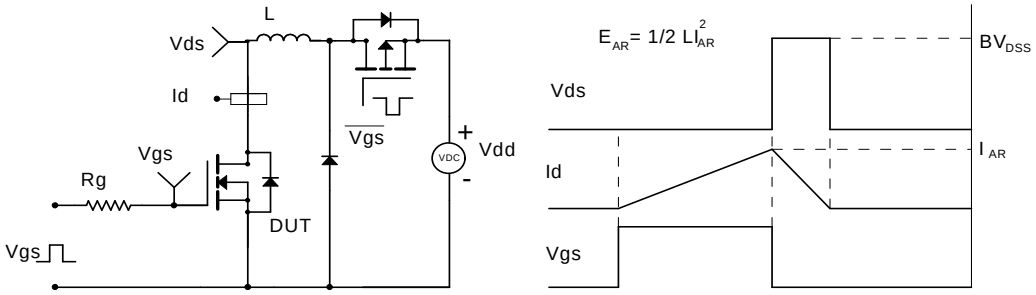
## Gate Charge Test Circuit & Waveform




## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms