VN920PEP-E

Single channel high side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920PEP-E	15 mΩ	30 A	36 V

- CMOS compatible input
- Proportional load current sense
- Shorted load protection
- Under voltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Protection against loss of ground and loss of V_{CC}
- Very low standby power dissipation
- Reverse battery protected (see *Application schematic on page 17*)
- In compliance with the 2002/95/ec european directive

PowerSSO-24

Description

The VN920PEP-E is a monolithic device designed in STMicroelectronics VIPower™ M0-3 technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility able).

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device integrates an analog current sense output which delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VN920PEP-E	VN920PEPTR-E

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

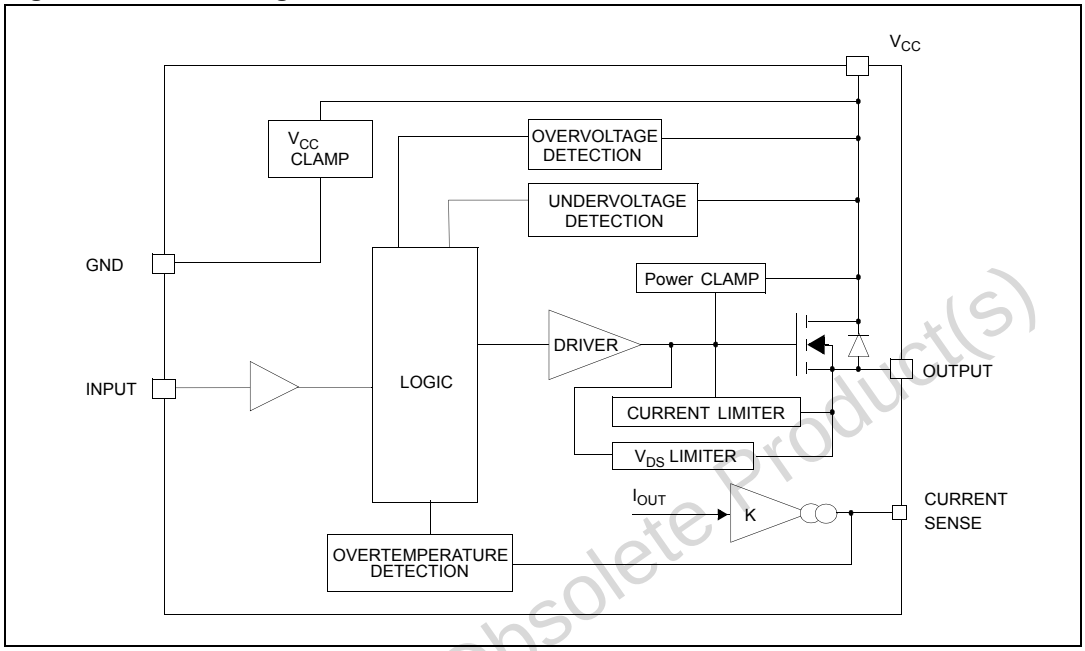


Figure 2. Configuration diagram (top view)

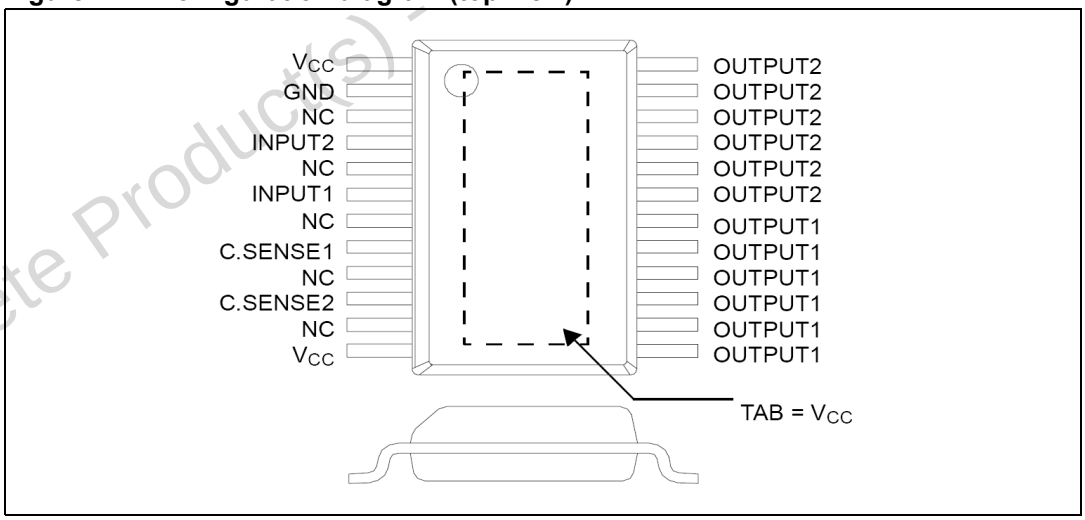
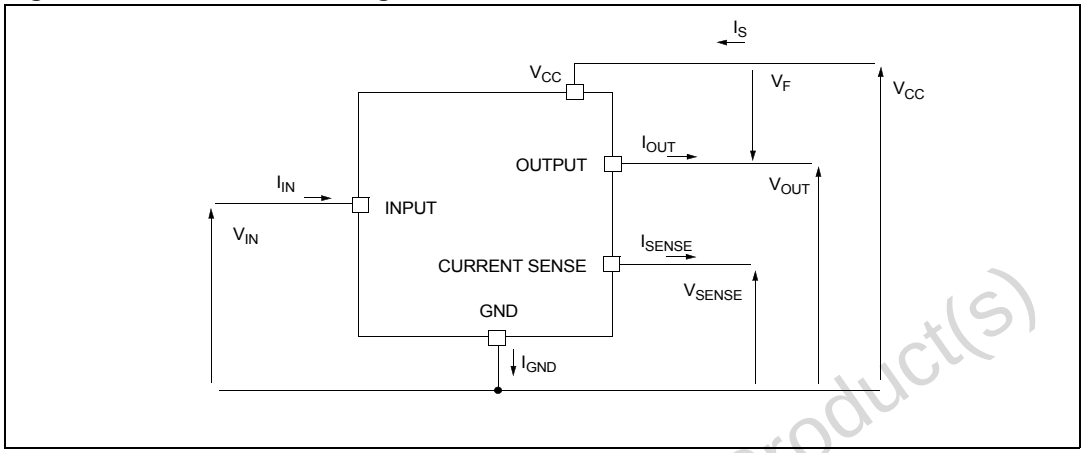


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	- 0.3	V
- I_{gnd}	DC reverse ground pin current	- 200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	- 40	A
I_{IN}	DC input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	- 3 + 15	V V
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ; C = 100pF) – Input – Current sense – Output – V_{CC}	 4000 2000 5000 5000	 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (L = 0.3mH; R_L= 0Ω; V_{bat} = 13.5V; T_{jstart} = 150°C; I_L = 45A)	462	mJ
P_{tot}	Power dissipation $T_C \leq 25°C$	8.3	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (max)	1.3		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max)	55(1)	40(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick).
2. When mounted on a standard single-sided FR-4 board with 8cm^2 of Cu (at least 35Éµm thick).

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 10A; T_j = 25°C; I_{OUT} = 10A; I_{OUT} = 3A; V_{CC} = 6V			15 30 50	mΩ mΩ mΩ
V_{CLAMP}	Clamp voltage	I_{CC} = 20mA(1)	41	48	55	V

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V		10	25	µA
		Off-state; V_{CC} = 13V; V_{IN} = V_{OUT} = 0V; T_j = 25°C		10	20	µA
		On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0A; R_{SENSE} = 3.9 kΩ			5	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = V_{SENSE}= 0V	0		50	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = V_{SENSE} = 0V; V_{CC} = 13V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = V_{SENSE} = 0V; V_{CC} = 13V; T_j = 25°C			3	µA

1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching (V_{CC}=13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3Ω (see *Figure 5*)		50		µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3Ω (see *Figure 5*)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 1.3Ω (see *Figure 5*)	See *Figure 16*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 1.3Ω (see *Figure 5*)	See *Figure 17*			V/µs

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high-level voltage		3.25			V
I_{IH}	High-level input current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = - 1mA	6	6.8 - 0.7	8	V V

Table 8. Current sense ($9V \le V_{CC} \le 16V$)(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1A; V_{SENSE} = 0.5V; T_j = -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT} = 1A; V_{SENSE} = 0.5V; T_j= - 40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10A; V_{SENSE} = 4V; T_j = - 40°C T_j= 25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 10A; V_{SENSE} = 4V; T_j = -40°C...150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 30A; V_{SENSE} = 4V; T_j = -40°C T_j = 25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 30A; V_{SENSE} = 4V; T_j = -40°C...150°C	-6		+6	%
I_{SENSE0}	Analog sense leakage current	V_{CC} = 6...16V; I_{OUT} = 0A; V_{SENSE} = 0V; T_j = -40°C...150°C	0		10	µA
V_{SENSE}	Max analog sense output voltage	V_{CC} = 5.5V; I_{OUT} = 5A; R_{SENSE} = 10kΩ V_{CC} > 8V, I_{OUT} = 10A; R_{SENSE} = 10kΩ	2 4			V V
V_{SENSEH}	Sense voltage in over temperature condition	V_{CC} = 13V; R_{SENSE} = 3.9kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in over temperature condition	V_{CC} = 13V; $T_j > T_{TSD}$; output open		400		Ω
t_{DSENSE}	Current sense delay response	To 90% I_{SENSE}(2)			500	µs

1. See *Figure 4*.
2. Current sense signal delay after positive input slope.

Table 9. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
I_{lim}	DC short circuit current	V_{CC} = 13V 5V < V_{CC} < 36V	30	45	75 75	A A

Table 9. Protections(1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; V_{IN} = 0V; L = 6mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A; T_j = -40°C...150°C		50		mV

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 10. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 5A; T_j = 150°C	-	-	0.6	V

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

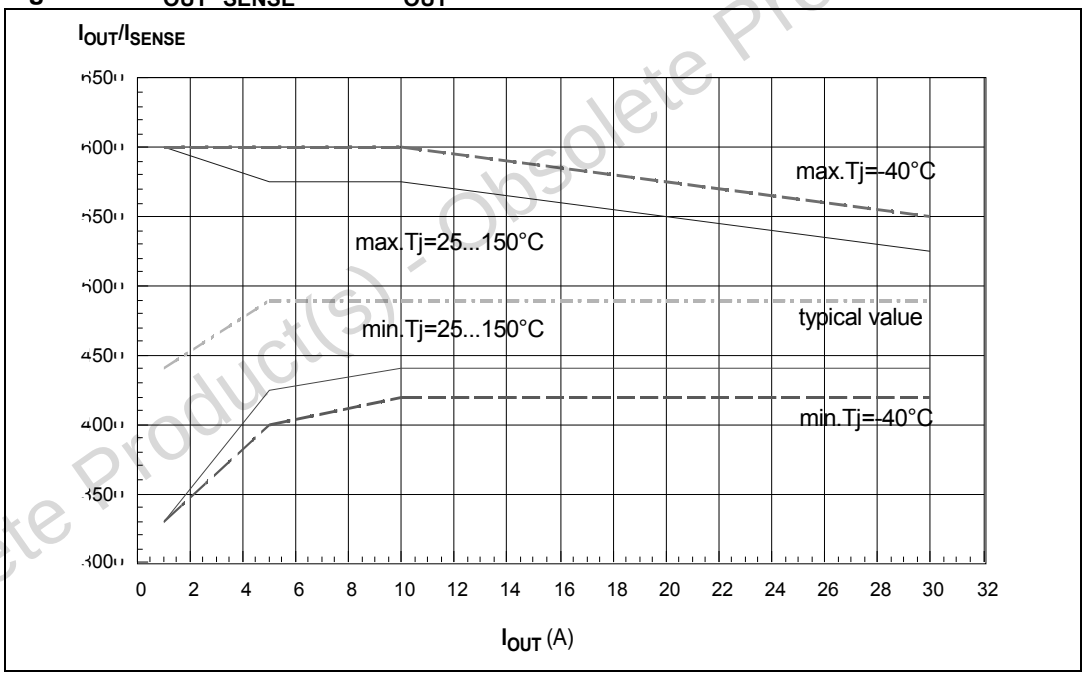


Figure 5. Switching characteristics

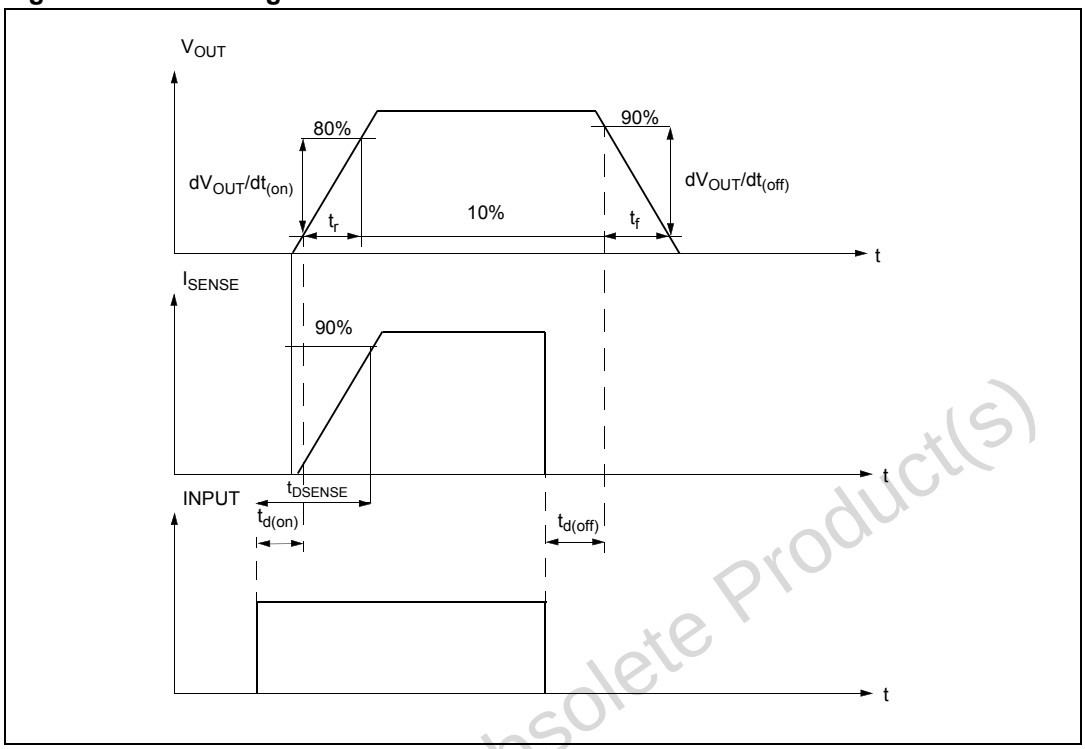


Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Over temperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Figure 6. Switching time waveforms

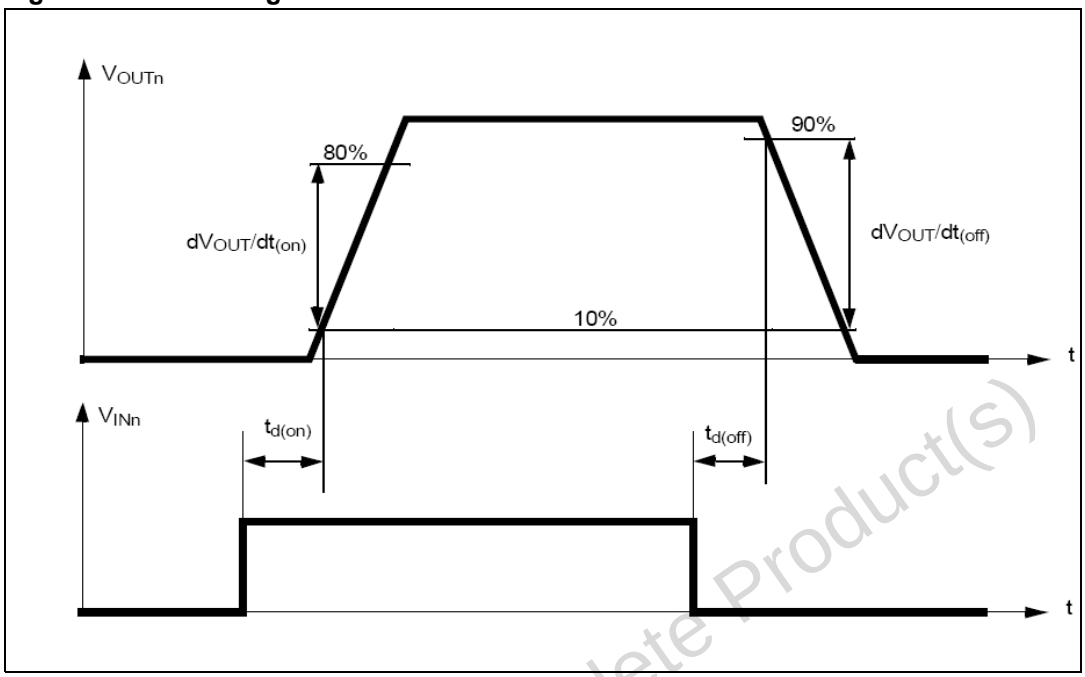


Table 12. Electrical transient requirements (part 1/3)

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1µs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1µs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

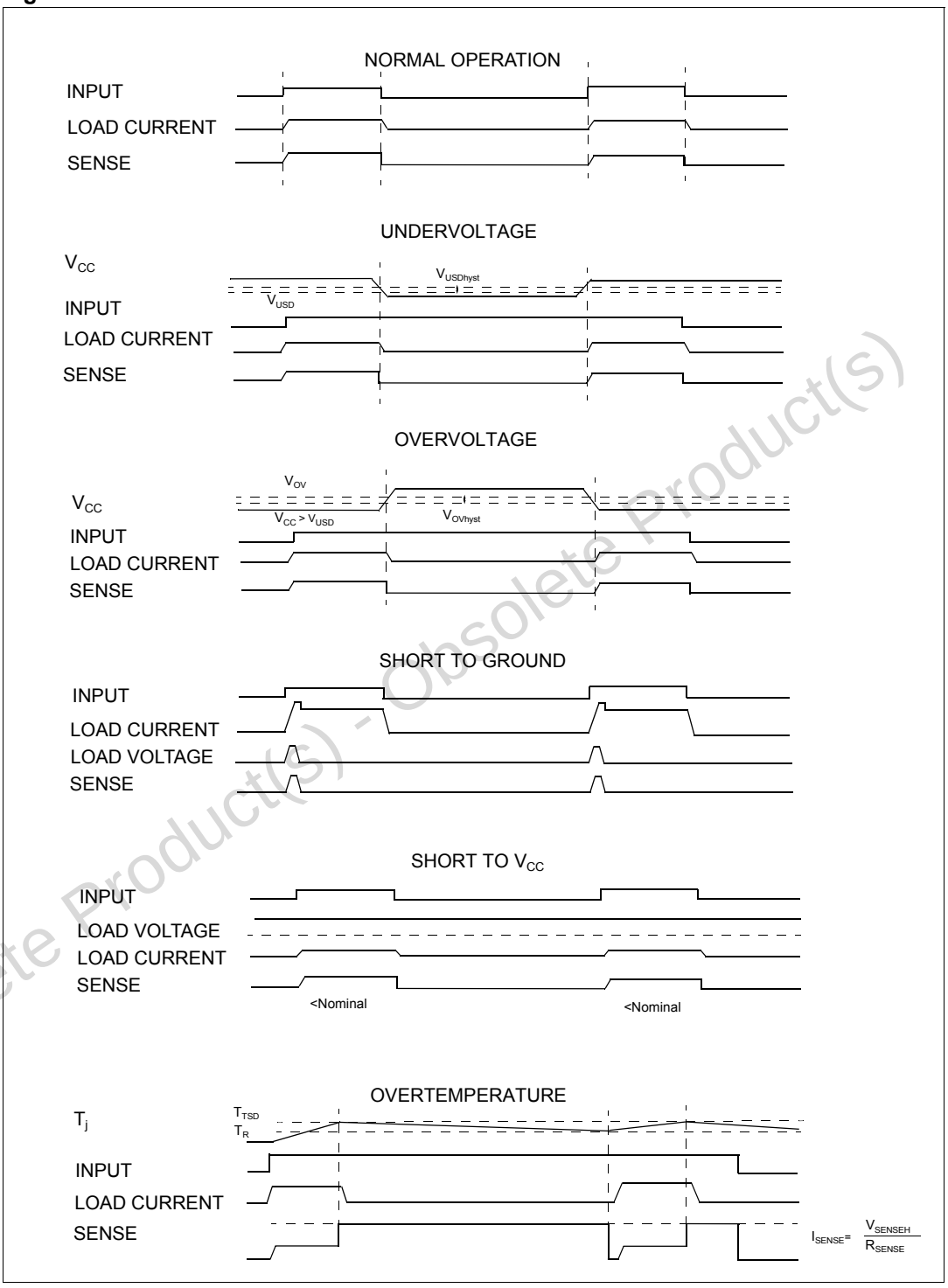
Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) Test pulse	Test level results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

Figure 7. Waveforms



2.4 Electrical characteristics curves

Figure 8. Off-state output current

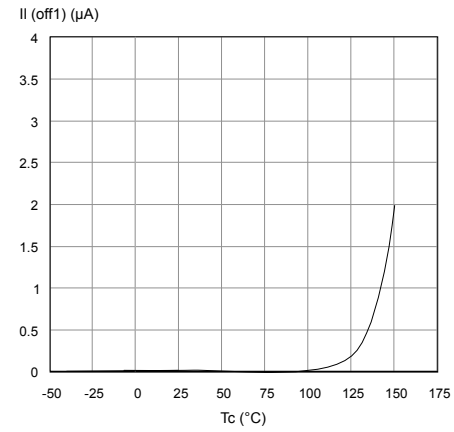


Figure 9. High level input current

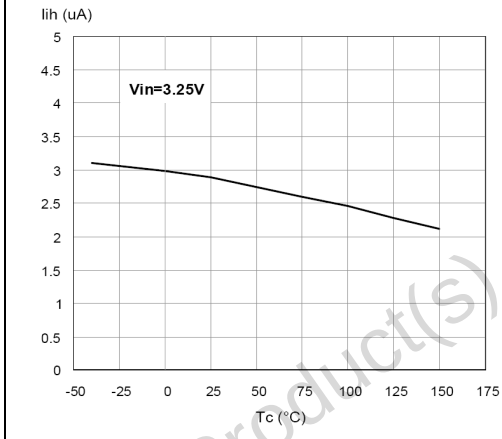


Figure 10. Input clamp voltage

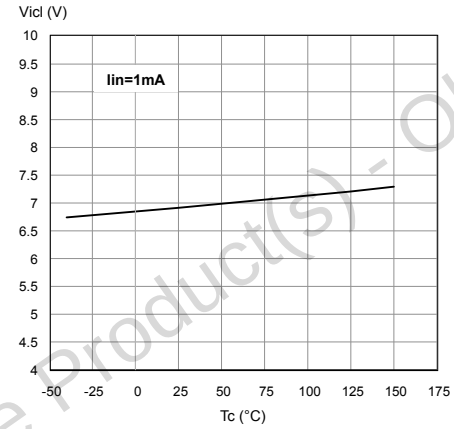


Figure 11. Input high level voltage

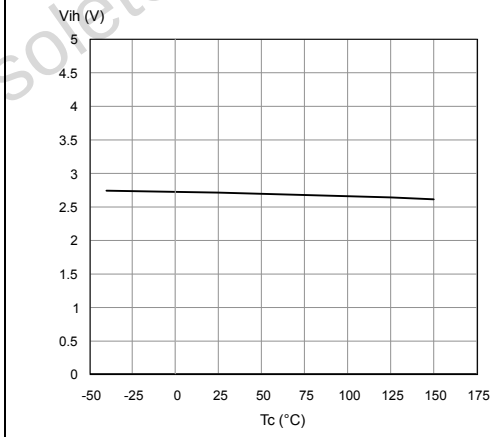


Figure 12. Input low level voltage

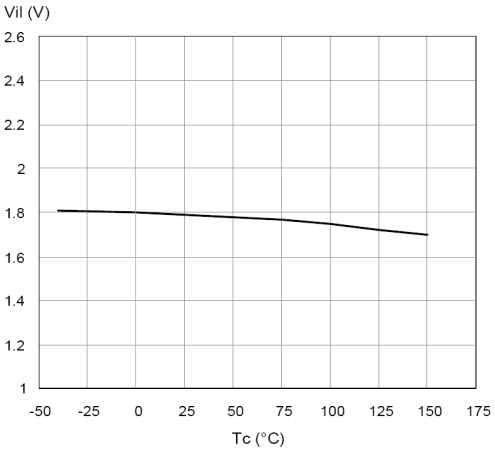


Figure 13. Input hysteresis voltage

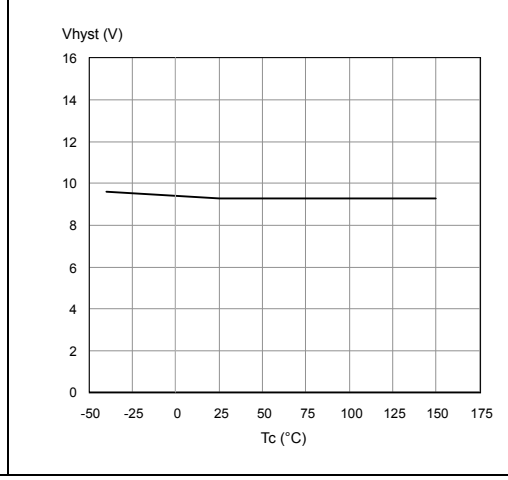


Figure 14. Overvoltage shutdown

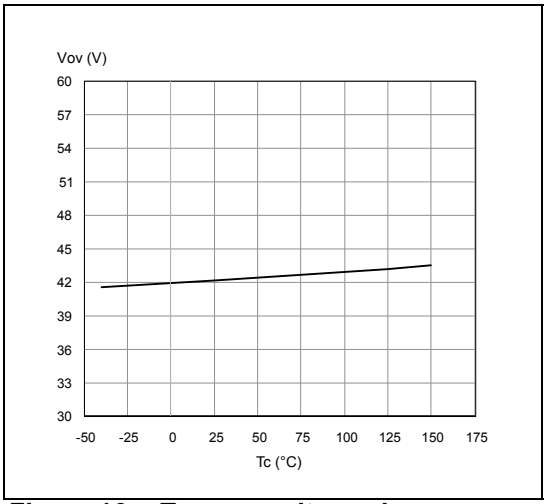


Figure 15. I_{LIM} vs T_{case}

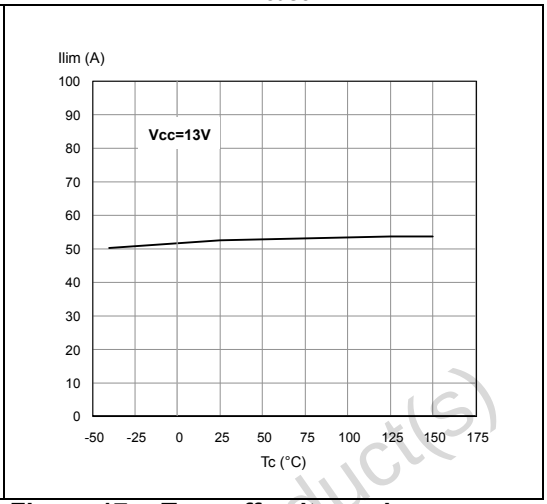


Figure 16. Turn-on voltage slope

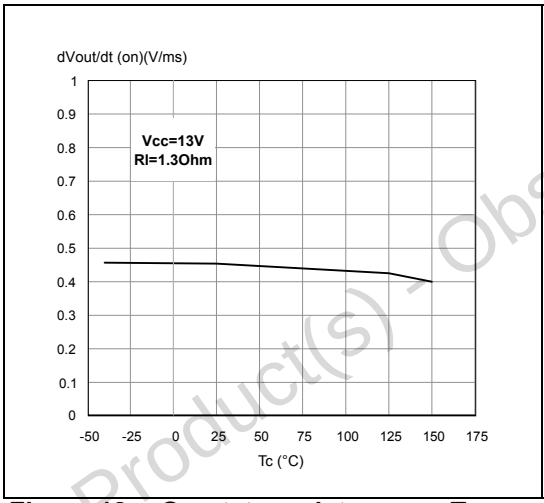


Figure 17. Turn-off voltage slope

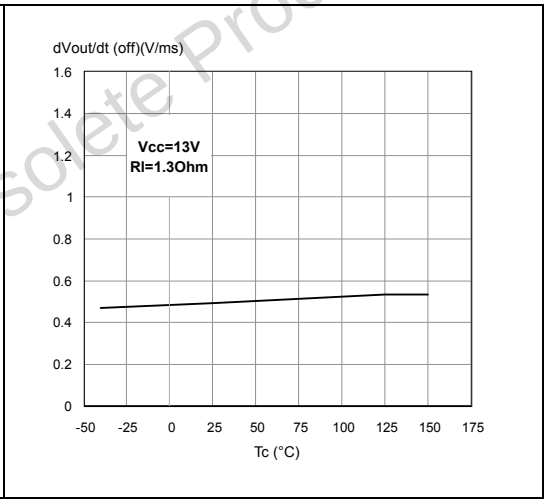
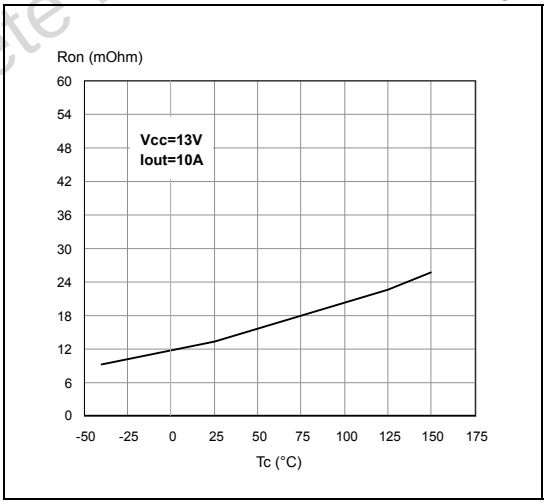
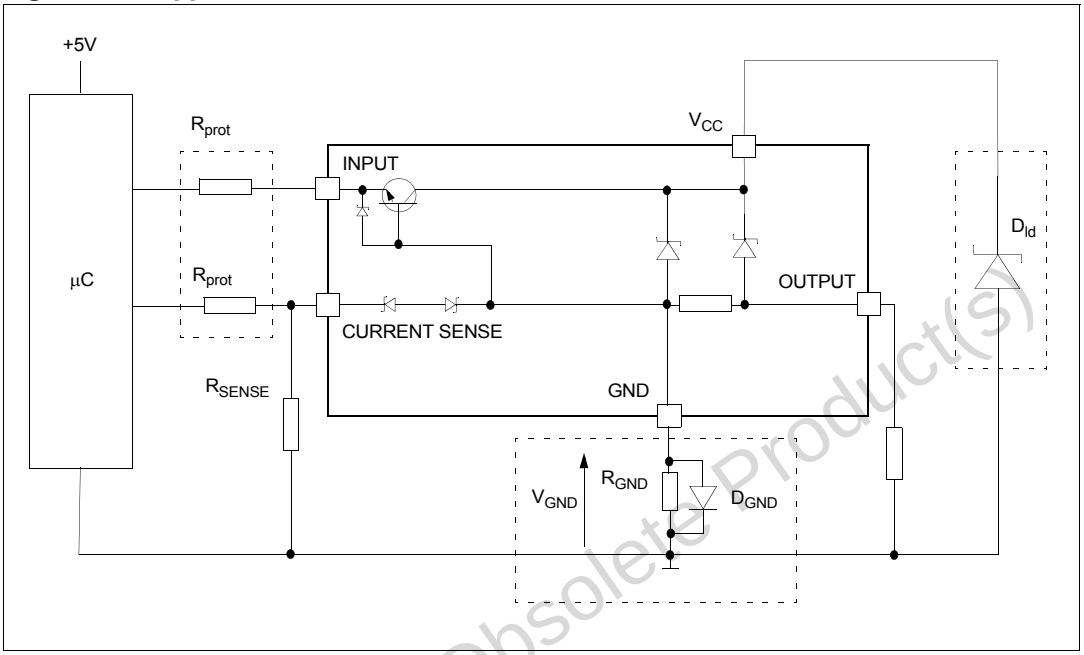


Figure 18. On-state resistance vs T_{CASE}



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where $- I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (- V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to ground pin.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

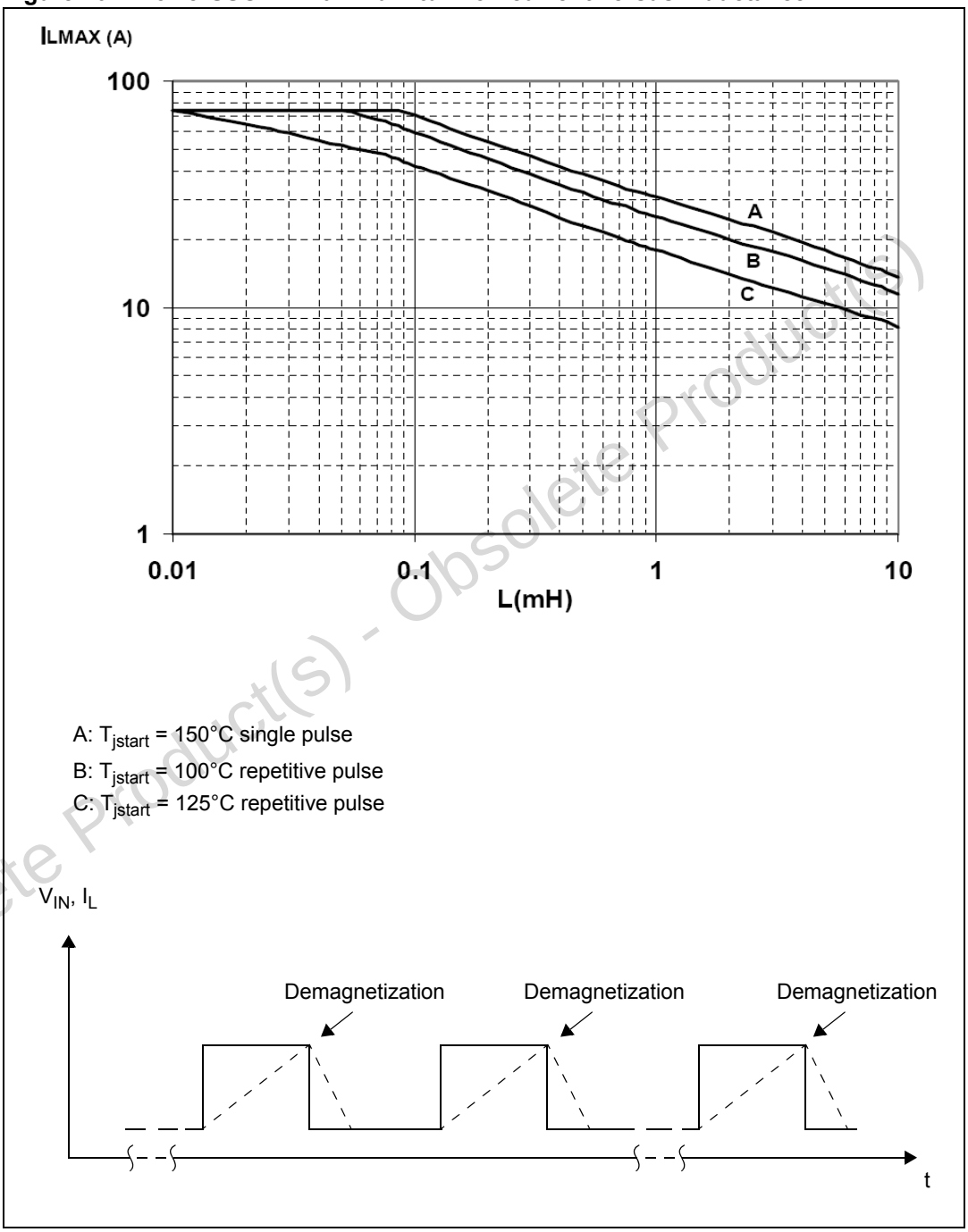
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended values: R_{prot} =10kΩ.

3.4 PowerSSO-24 maximum demagnetization energy (V_{CC}=13.5V)

Figure 20. PowerSSO-24 maximum turn-off current versus inductance

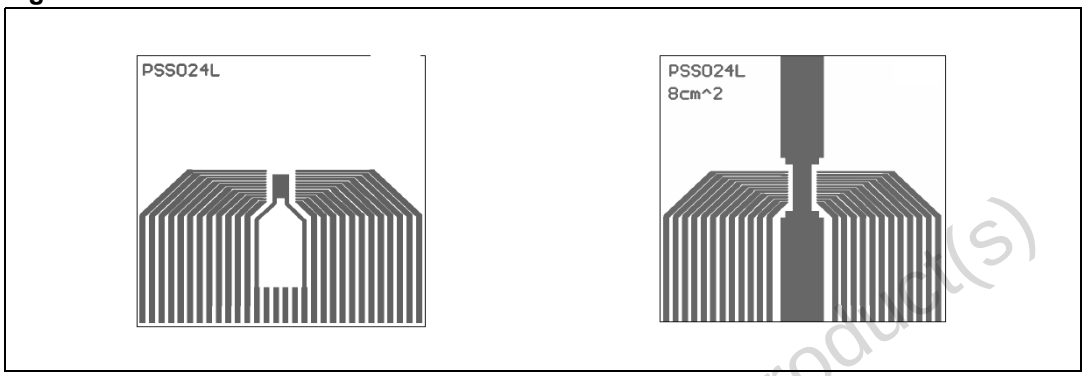


$_L\Omega$.In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-24 thermal data

Figure 21. PowerSSO-24 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 78mm x 78mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: from minimum pad layout to 8cm^2).

Figure 22. PowerSSO-24 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

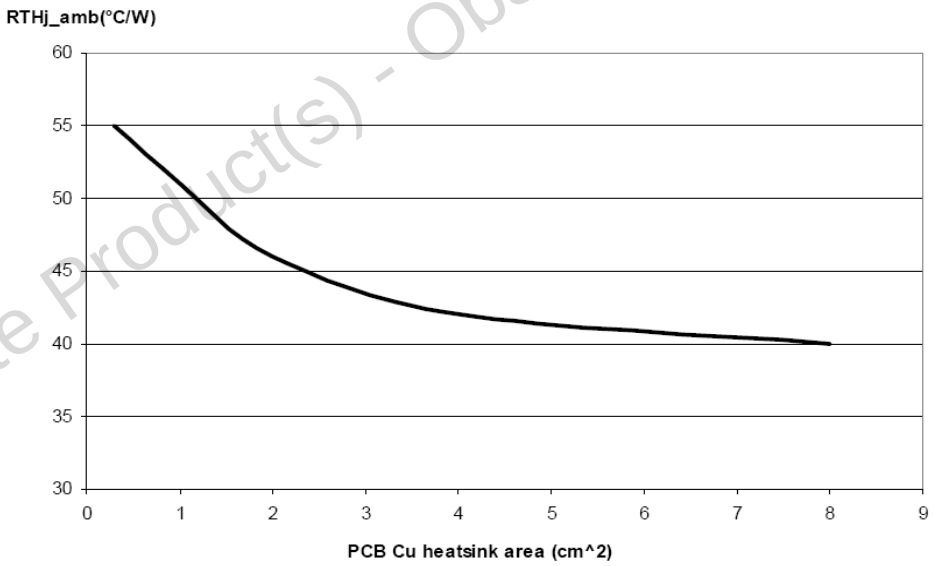
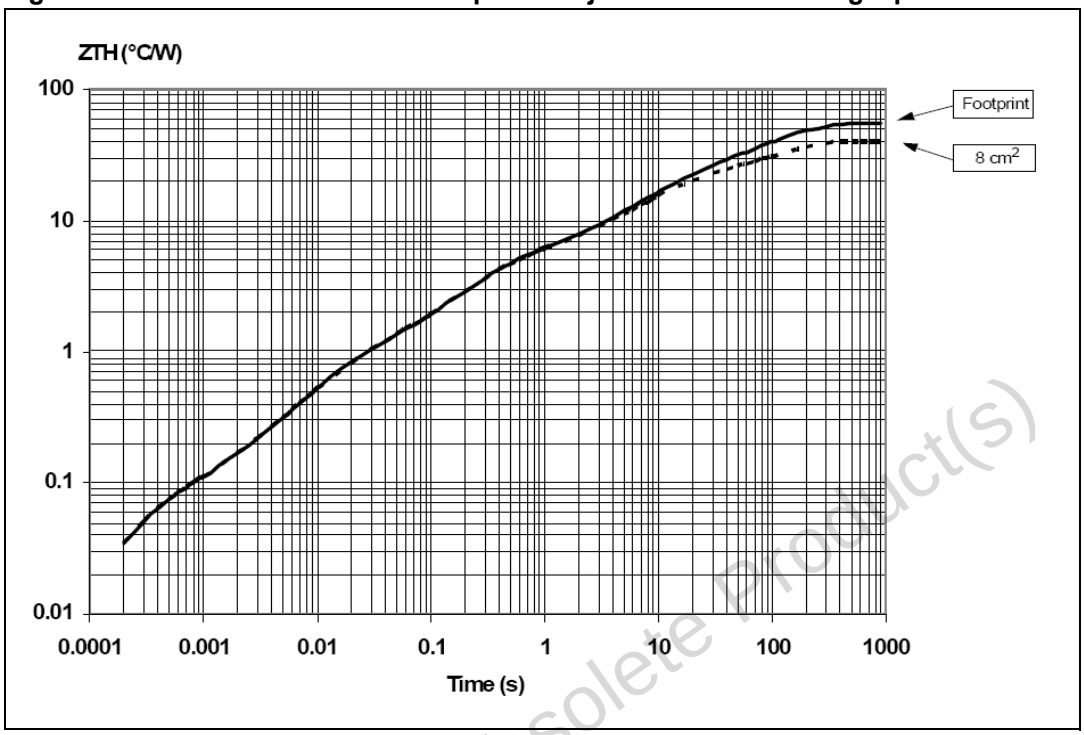


Figure 23. PowerSSO-24 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p/T$

Figure 24. Thermal fitting model of a single channel HSD in PowerSSO-24

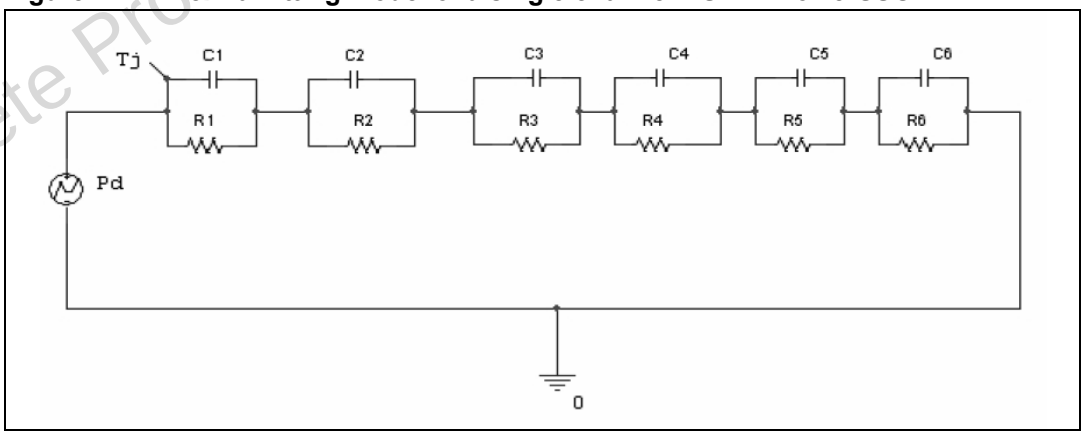


Table 15. PowerSSO-24 thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.012	
R2 (°C/W)	0.05	

Table 15. PowerSSO-24 thermal parameters (continued)

R3 (°C/W)	0.65	
R4 (°C/W)	4	
R5 (°C/W)	13.5	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0004	
C2 (W.s/°C)	0.005	
C3 (W.s/°C)	0.022	
C4 (W.s/°C)	0.08	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 25. PowerSSO-24 package dimensions

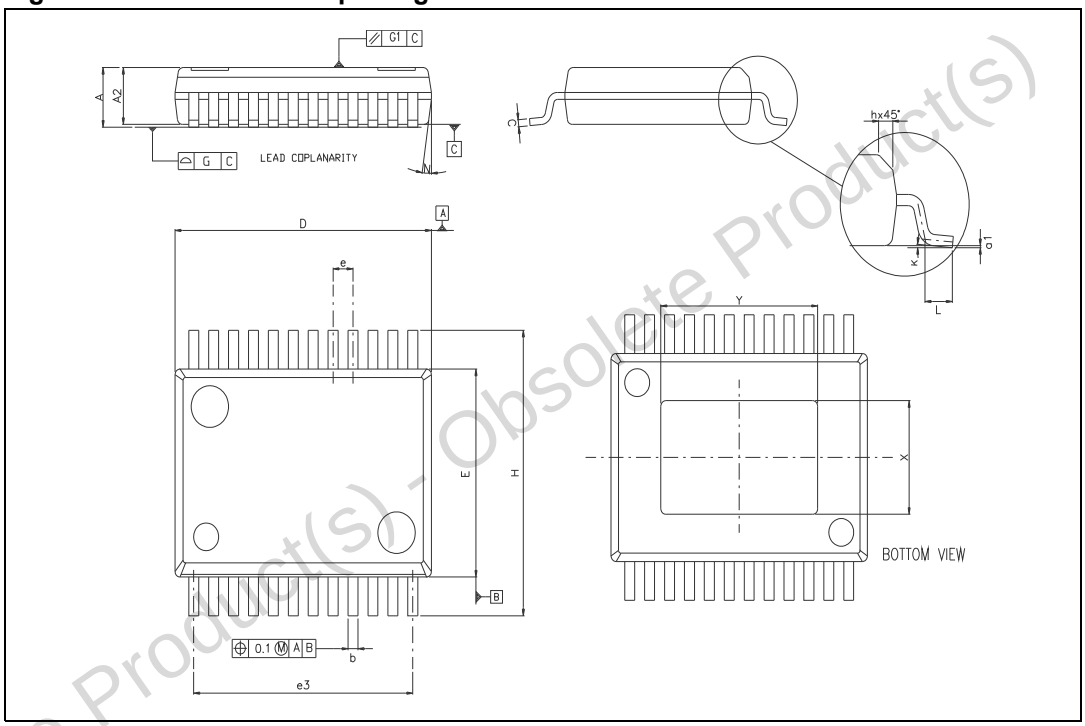


Table 16. PowerSSO-24™ mechanical data

Symbol	millimeters		
	Min	Typ	Max
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	

Table 16. PowerSSO-24™ mechanical data (continued)

Symbol	millimeters		
	Min	Typ	Max
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

6 Revision history

Table 17. Document revision history

Date	Revision	Changes
22-Oct-2004	1	Initial release.
07-Nov-2004	2	Mechanical data updating. PowerSSO-24 thermal characteristics insertion
09-Dec-2004	3	PC Board copper area correction.
15-Dec-2004	4	- IL(off2) removal.
17-Mar-2005	5	– Maximum switching energy value insertion. – Maximum turn off current versus load inductance curve insertion. – Minor changes.
01-Jul-2009	6	*Table 16: PowerSSO-24™ mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows
20-Sep-2013	7	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com