

## MPC823 AC Electrical Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC823.



**Note:** Visit our website at [www.freescale.com](http://www.freescale.com) if you are using a frequency other than 25, 40, or 50MHz. Our website contains a spreadsheet that you can use to calculate the timing for your specific system frequency.

This device contains circuitry protecting against damage from high-static voltage or electrical fields. However, it is advised that precautions be taken to avoid application of any voltages higher than the maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or  $V_{CC}$ ).

**MAXIMUM RATINGS (GND = 0V)**

| RATING   | SYMBOL           | VALUE                         | UNIT |
|--|------------------|-------------------------------|------|
| Supply Voltage   | VDDH             | -0.3 to 4.0                   | V    |
|  | VDD              | -0.3 to 4.0                   | V    |
|  | KAPWR            | -0.3 to 4.0                   | V    |
|  | VDDSYN           | -0.3 to 4.0                   | V    |
| Input Voltage (JTAG and GPIO)  | VIN              | -0.3 to 5.8                   | V    |
| Input Voltage (All other pins)   | VIN              | -0.3 to 3.3                   | V    |
| Operating Temperature  | T <sub>A</sub>   | 0 to 70°<br>or<br>-40° to 85° | °C   |
| Storage Temperature Range  | T <sub>STG</sub> | -55 to +150                   | °C   |
| <p>NOTES:</p> <ol style="list-style-type: none"> <li>Functional operating conditions are given in <b>DC Electrical Characteristics (VCC = 3.0 - 3.6 V)</b>. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.</li> <li><b>CAUTION:</b> The JTAG and GPIO input voltages cannot be more than 2.5 V greater than supply voltage, this restriction applies also on “power-on” as well as on normal operation.</li> <li>5 Volt friendly inputs are inputs that tolerate 5 volts for JTAG and GPIO pins.</li> <li>If you are using Mask Revision Base #F98S (Revision 0), all pins except EXTAL and CLK4IN are 5V tolerant inputs.</li> </ol> |                  |                               |      |

**THERMAL CHARACTERISTICS**

| CHARACTERISTIC             | SYMBOL        | VALUE | UNIT |
|----------------------------|---------------|-------|------|
| Thermal Resistance for BGA | $\theta_{Jc}$ | ~30   | °C/W |

**POWER CONSIDERATIONS**

The average chip-junction temperature,  $T_J$ , in °C can be obtained from

$$T_J = T_A + (P_D \cdot q_{JA}) \quad (1)$$

where

- $T_A$  = Ambient Temperature, °C
- $q_{JA}$  = Package Thermal Resistance, Junction to Ambient, °C/W
- $P_D$  =  $P_{INT} + P_{I/O}$
- $P_{INT}$  =  $I_{DD} \times V_{DD}$ , Watts—Chip Internal Power
- $P_{I/O}$  = Power Dissipation on Input and Output Pins—User Determined

For most applications  $P_{I/O} < 0.3 \cdot P_{INT}$  and can be neglected. If  $P_{I/O}$  is neglected, an approximate relationship between  $P_D$  and  $T_J$  is:

$$P_D = K \Pi (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives

$$K = \frac{P_D \cdot (T_A + 273^\circ\text{C}) + q_{JA} \cdot P_D^2}{T_J + 273^\circ\text{C}} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_J$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

**Layout Practices**

Each  $V_{CC}$  pin on the MPC823 should be provided with a low-impedance path to the board's supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{CC}$  power supply should be bypassed to ground using at least four 0.1  $\mu\text{F}$  bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{CC}$  and GND should be kept to less than half an inch per capacitor lead. A four-layer board that employs two inner layers as  $V_{CC}$  and GND planes should be used.

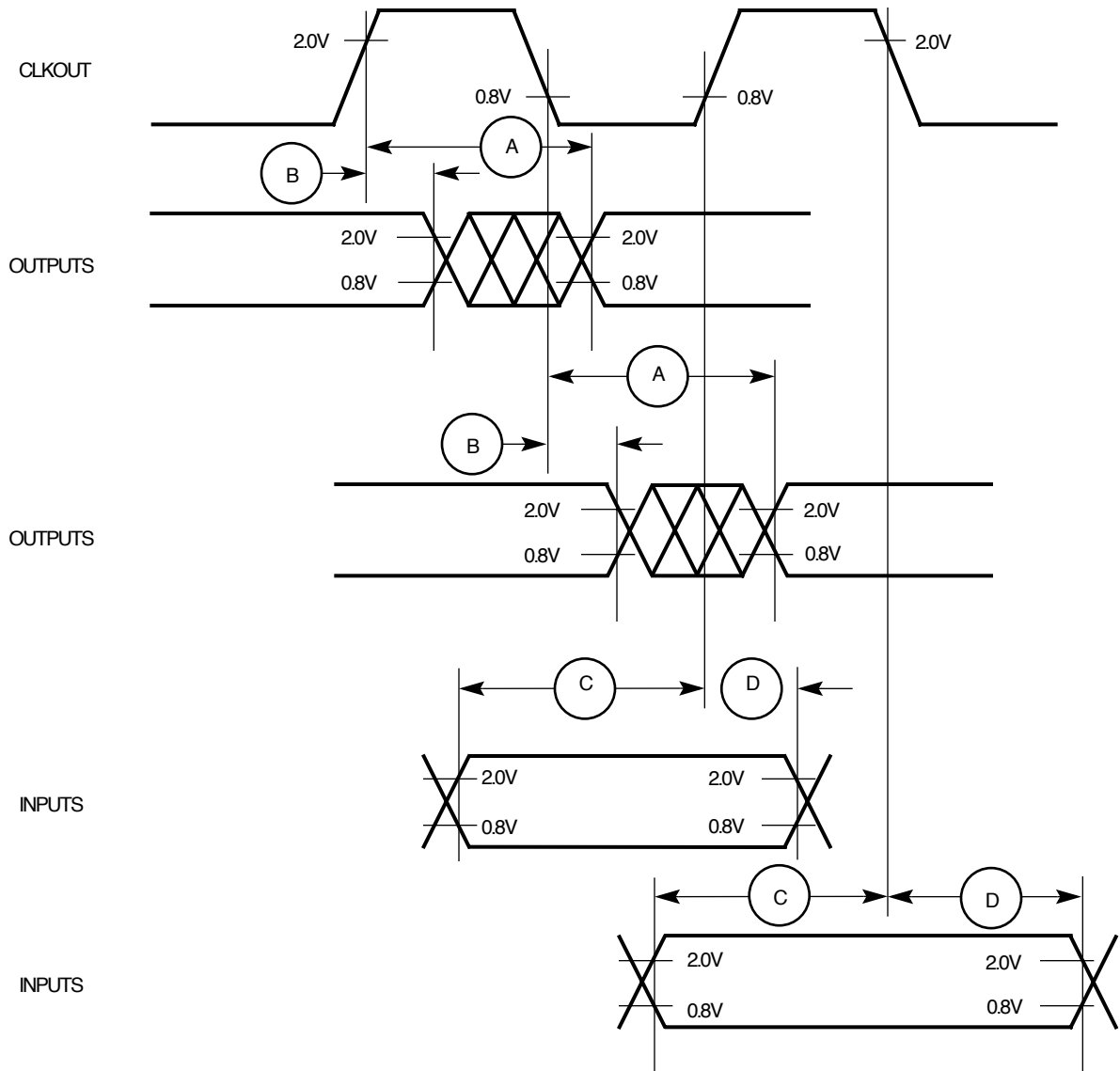
All output pins on the MPC823 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 3.0 - 3.6 V$ )

| CHARACTERISTIC  | SYMBOL    | MIN            | MAX          | UNIT    |
|---|-----------|----------------|--------------|---------|
| Input High Voltage (for JTAG and GPIO)  | $V_{IH}$  | 2.0            | 5.5          | V       |
| Input High Voltage (all other pins)   | $V_{IH}$  | 2.0            | 3.6          | V       |
| Input Low Voltage   | $V_{IL}$  | GND            | 0.8          | V       |
| EXTAL and EXTCLK Input High Voltage   | $V_{IHC}$ | $0.7*(V_{CC})$ | $V_{CC}+0.3$ | V       |
| Input Leakage Current, $V_{IN} = 5.5 V$   | $I_{IN}$  | —              | $\pm 10$     | $\mu A$ |
| Hi-z (Off State) Leakage Current, $V_{IN} = 3.5V$   | $I_{OZ}$  | —              | $\pm 10$     | $\mu A$ |
| Signal Low Input Current, $V_{IL} = 0.8 V$  | $I_L$     |                | $\pm 10$     | $\mu A$ |
| Signal High Input Current, $V_{IH} = 2.0 V$   | $I_H$     |                | $\pm 10$     | $\mu A$ |
| Output High Voltage, $I_{OH} = -2.0 mA$ , $V_{DDH} = 3.0V$<br>Except XTAL, XFC, and Open-Drain Pins   | $V_{OH}$  | 2.4            | —            | V       |
| Output Low Voltage<br>$I_{OL} = 2.0 mA$ CLKOUT<br>$I_{OL} = 3.2 mA$ A[6:31], TSIZ0/REG, TSIZ1, D[0:31], DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, USBRXD/PA15, RXD2/PA13, SMRXD2/L1TXDA/PA9, SMTXD2/L1RXDA/PA8, IRQ4/KR/SPKROUT, TIN1/L1RCLKA/BRGO1/CLK1/PA7, TIN3/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TIN4/TOUT2/CLK4/PA4, LCD_A/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO3/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, LCD_B/L1ST1/PB19, L1ST2/RTS2/PB18, LCD_C/L1ST3/PB17, L1ST4/L1RQA/PB16, L1ST5/DREQ1/PC15, L1ST6/RTS2/DREQ2/PC14, L1ST7/PC13, L1ST8/L1RQA/PC12, USBRXP/PC11, USBRXN/TGATE1/PC10, CTS2/PC9, TGATE1/CD2/PC8, USBTXP/PC7, USBTXN/PC6, SDACK1/L1TSYNCA/PC5, L1RSYNCA/PC4, LD8/VD7/PD15, LD7/VD6/PD14, LD6/VD5/PD13, LD5/VD4/PD12, LD4/VD3/PD11, LD3/VD2/PD10, LD2/VD1/PD9, LD1/VD0/PD8, FRAME/VSYNCPD5, LCD_AC/LOE/BLANK/PD6, LD0/FIELD/PD7, LOAD/HSYNCPD4, SHIFT/CLK/PD3 | $V_{OL}$  | —              | 0.5          | V       |
| $I_{OL} = 5.3 mA$ BDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO<br>$I_{OL} = 7.0 mA$ USBOE/PA14, TXD2/PA12<br>$I_{OL} = 8.9 mA$ TS, TA, TEA, BI, BB, HRESET, SRESET  |           |                |              |         |

NOTE: Input pin voltage specifications are  $V_{CC} = +4 V$  or  $5.8 V$ , whichever is less.  
AC timings are based on a  $50 pF$  load.  
If you are using Mask Revision Base #F98S, all pins except EXTAL and CLK4IN are 5V tolerant inputs.

AC ELECTRICAL CHARACTERISTICS



|                                      |  |
|--------------------------------------|--|
| A=MAXIMUM OUTPUT DELAY SPECIFICATION | C=MINIMUM INPUT SETUP TIME SPECIFICATION |
| B=MINIMUM OUTPUT HOLD TIME           | D=MINIMUM INPUT HOLD TIME SPECIFICATION  |

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EXTERNAL BUS ELECTRICAL CHARACTERISTICS

Table 1. Bus Operation Timing

| NUM  | CHARACTERISTIC  | 25MHz |     | 40MHz |       | 50MHz |       | UNIT |
|------|---|-------|-----|-------|-------|-------|-------|------|
|      |   | MIN   | MAX | MIN   | MAX   | MIN   | MAX   |      |
| B1   | CLKOUT Period   | 40    | —   | 25    | —     | 20    | —     | ns   |
| B1a  | EXTCLK to CLKOUT Phase Skew (EXTCLK>15MHz and MF ≤ 2)                                     | -0.9  | 0.9 | -0.9  | 0.9   | -0.9  | 0.9   | ns   |
| B1b  | EXTCLK to CLKOUT Phase Skew (EXTCLK>10MHz and MF ≤ 10)                                    | -2.3  | 2.3 | -2.3  | 2.3   | -2.3  | 2.3   | ns   |
| B1c  | CLKOUT Phase Jitter (EXTCLK>15MHz and MF≤2)   | -0.6  | 0.6 | -0.6  | 0.6   | -0.6  | 0.6   | ns   |
| B1d  | CLKOUT Phase Jitter (EXTCLK>10MHz and MF≤10)  | -2    | 2   | -2    | 2     | -2    | 2     | ns   |
| B1e  | CLKOUT Frequency Jitter (MF<10)   | —     | 0.5 | —     | 0.5   | —     | 0.5   | %    |
| B1f  | CLKOUT Frequency Jitter (10<MF<500)   | —     | 2   | —     | 2     | —     | 2     | %    |
| B1g  | CLKOUT Frequency Jitter (MF>500)  | —     | 3   | —     | 3     | —     | 3     | %    |
| B1h  | Frequency Jitter on EXTCLK  | —     | 0.5 | —     | 0.5   | —     | 0.5   | %    |
| B2   | Clock Pulse Width Low   | 16    | —   | 10    | —     | 8     | —     | ns   |
| B3   | Clock Pulse Width High  | 16    | —   | 10    | —     | 8     | —     | ns   |
| B4   | CLKOUT Rise Time  | —     | 4   | —     | 4     | —     | 4     | ns   |
| B5   | CLKOUT Fall Time  | —     | 4   | —     | 4     | —     | 4     | ns   |
| B6   | N/A (Used on Interactive Spreadsheet)   |       |     |       |       |       |       |      |
| B7   | CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP(0:3) Invalid                                 | 10    | —   | 5     | —     | 5     | —     | ns   |
| B7a  | CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR Invalid                                 | 10    | —   | 5     | —     | 5     | —     | ns   |
| B7b  | CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), STS Invalid                | 10    | —   | 5     | —     | 5     | —     | ns   |
| B8   | CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP(0:3) Valid                                   | 10    | 19  | 5     | 13    | 5     | 12    | ns   |
| B8a  | CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR Valid                                   | 10    | 19  | 5     | 13    | 5     | 12    | ns   |
| B8b  | CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid                  | 10    | 19  | 5     | 13    | 5     | 12    | ns   |
| B9   | CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR Hi Z | 10    | 19  | 5     | 13    | 5     | 12    | ns   |
| B10  | N/A   |       |     |       |       |       |       |      |
| B11  | CLKOUT to TS, BB Assertion  | 10    | 19  | 5     | 12.25 | 5     | 12.25 | ns   |
| B11a | CLKOUT to TA, BI Assertion (when driven by the Memory Controller or PCMCIA Interface)     | 2.5   | 11  | 2.5   | 9.25  | 2.5   | 9.25  | ns   |
| B12  | CLKOUT to TS, BB Negation   | 10    | 19  | 5     | 13    | 5     | 12    | ns   |
| B12a | CLKOUT to TA, BI Negation (when driven by the Memory Controller or PCMCIA Interface)      | 2.5   | 11  | 2.5   | 11    | 2.5   | 11    | ns   |
| B13  | CLKOUT to TS, BB Hi Z   | 10    | 24  | 5     | 21    | 5     | 19    | ns   |

**Table 1. Bus Operation Timing (Continued)**

| NUM  | CHARACTERISTIC   | 25MHz |     | 40MHz |     | 50MHz |     | UNIT |
|------|--|-------|-----|-------|-----|-------|-----|------|
|      |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| B13a | CLKOUT to $\overline{TA}$ , $\overline{BI}$ Hi Z (When Driven by the Memory Controller or PCMCIA Interface)                            | 2.5   | 15  | 2.5   | 15  | 2.5   | 16  | ns   |
| B14  | CLKOUT to $\overline{TEA}$ Assertion   | 2.5   | 11  | 2.5   | 11  | 2.5   | 10  | ns   |
| B15  | CLKOUT to $\overline{TEA}$ Hi Z  | 2.5   | 15  | 2.5   | 15  | 2.5   | 15  | ns   |
| B16  | $\overline{TA}$ , $\overline{BI}$ Valid to CLKOUT (Setup Time)   | 9.75  | —   | 9.75  | —   | 9.75  | —   | ns   |
| B16a | $\overline{TEA}$ , $\overline{KR}$ , $\overline{RETRY}$ Valid to CLKOUT (Setup Time)   | 11    | —   | 10    | —   | 10    | —   | ns   |
| B16b | $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ Valid to CLKOUT (Setup Time)   | 8.5   | —   | 8.5   | —   | 8.5   | —   | ns   |
| B17  | CLKOUT to $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ Valid (Hold Time) | 1     | —   | 1     | —   | 1     | —   | ns   |
| B17a | CLKOUT to $\overline{KR}$ , $\overline{RETRY}$ Valid (Hold Time)   | 2     | —   | 2     | —   | 2     | —   | ns   |
| B18  | D(0:31), DP(0:3) Valid to CLKOUT Rising Edge (Setup Time)  | 6     | —   | 6     | —   | 6     | —   | ns   |
| B19  | CLKOUT Rising Edge to D(0:31), DP(0:3) Valid (Hold Time)   | 2     | —   | 2     | —   | 2     | —   | ns   |
| B20  | D(0:31), DP(0:3) Valid to CLKOUT Falling Edge (Setup Time)   | 4     | —   | 4     | —   | 4     | —   | ns   |
| B21  | CLKOUT Falling Edge to D(0:31), DP(0:3) Valid (Hold Time)  | 2     | —   | 2     | —   | 2     | —   | ns   |
| B22  | CLKOUT Rising Edge to $\overline{CS}$ Asserted -GPCM- ACS = 00   | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B22a | CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0  | —     | 10  | —     | 8   | —     | 8   | ns   |
| B22b | CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 0  | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B22c | CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1  | 14    | 25  | 7     | 16  | 7     | 16  | ns   |
| B23  | CLKOUT Rising Edge to $\overline{CS}$ Negated -GPCM-Read Access - GPCM-Write Access, ACS=00, TRLX=0, CSNT=0                            | 3     | 10  | 2     | 8   | 2     | 8   | ns   |
| B24  | A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0  | 8     | —   | 3     | —   | 3     | —   | ns   |
| B24a | A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0  | 18    | —   | 8     | —   | 8     | —   | ns   |
| B25  | CLKOUT Rising Edge to $\overline{OE}$ , $\overline{WE}$ (0:3) Asserted   | —     | 11  | —     | 9   | —     | 9   | ns   |
| B26  | CLKOUT Rising Edge to $\overline{OE}$ Negated  | 3     | 11  | 2     | 9   | 2     | 9   | ns   |
| B27  | A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 1  | 48    | —   | 23    | —   | 23    | —   | ns   |
| B27a | A(6:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 1  | 58    | —   | 28    | —   | 28    | —   | ns   |
| B28  | CLKOUT Rising Edge to $\overline{WE}$ (0:3) Negated -GPCM-Write Access CSNT = '0'  | —     | 11  | —     | 9   | —     | 9   | ns   |
| B28a | CLKOUT Falling Edge to $\overline{WE}$ (0:3) Negated -GPCM-Write Access TRLX = '0', CSNT = '1', EBDF=0                                 | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B28b | CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0             | —     | 20  | —     | 13  | —     | 13  | ns   |

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## Table 1. Bus Operation Timing (Continued)

| NUM  | CHARACTERISTIC   | 25MHz |     | 40MHz |     | 50MHz |     | UNIT |
|------|--|-------|-----|-------|-----|-------|-----|------|
|      |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| B28c | CLKOUT Falling Edge to $\overline{WE}(0:3)$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', EBDF=1  | 14    | 25  | 7     | 16  | 7     | 16  | ns   |
| B28d | CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1   | —     | 25  | —     | 16  | —     | 16  | ns   |
| B29  | $\overline{WE}(0:3)$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, CSNT = '0'  | 8     | —   | 3     | —   | 3     | —   | ns   |
| B29a | $\overline{WE}(0:3)$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 0  | 18    | —   | 8     | —   | 8     | —   | ns   |
| B29b | $\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, ACS = '00', TRLX = '0' & CSNT = '0'  | 8     | —   | 3     | —   | 3     | —   | ns   |
| B29c | $\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0   | 18    | —   | 8     | —   | 8     | —   | ns   |
| B29d | $\overline{WE}(0:3)$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 0  | 58    | —   | 28    | —   | 28    | —   | ns   |
| B29e | $\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0   | 58    | —   | 28    | —   | 28    | —   | ns   |
| B29f | $\overline{WE}(0:3)$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 1  | 12    | —   | 5     | —   | 5     | —   | ns   |
| B29g | $\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1   | 12    | —   | 5     | —   | 5     | —   | ns   |
| B29h | $\overline{WE}(0:3)$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 1  | 52    | —   | 24    | —   | 24    | —   | ns   |
| B29i | $\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1   | 52    | —   | 24    | —   | 24    | —   | ns   |
| B30  | $\overline{CS}$ , $\overline{WE}(0:3)$ Negated to A(6:31) invalid -GPCM- Write Access.   | 8     | —   | 3     | —   | 3     | —   |      |
| B30a | $\overline{WE}(0:3)$ Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1'. $\overline{CS}$ Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='0', CSNT = '1', ACS = 10, ACS = '11', EBDF = 0 | 18    | —   | 8     | —   | 8     | —   | ns   |
| B30b | $\overline{WE}(0:3)$ Negated to A(6:31)Invalid -GPCM- Write Access, TRLX='1', CSNT = '1'. $\overline{CS}$ Negated to A(6:31)Invalid -GPCM-Write Access, TRLX='1', CSNT = '1', ACS = 10, ACS = '11', EBDF = 0   | 58    | —   | 28    | —   | 28    | —   | ns   |
| B30c | $\overline{WE}(0:3)$ Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1'. $\overline{CS}$ Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='0', CSNT = '1', ACS = 10 ,ACS = '11', EBDF = 1 | 12    | —   | 4     | —   | 4     | —   | ns   |
| B30d | $\overline{WE}(0:3)$ Negated to A(6:31) Invalid -GPCM- Write Access, TRLX='1', CSNT = '1'. $\overline{CS}$ Negated to A(6:31) Invalid -GPCM-Write Access, TRLX='1', CSNT = '1', ACS = 10,ACS = '11', EBDF = 1  | 52    | —   | 24    | —   | 24    | —   | ns   |
| B31  | CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST4 in the corresponding word of the UPM   | 1.5   | 10  | 1.5   | 8   | 1.5   | 8   | ns   |



## Table 1. Bus Operation Timing (Continued)

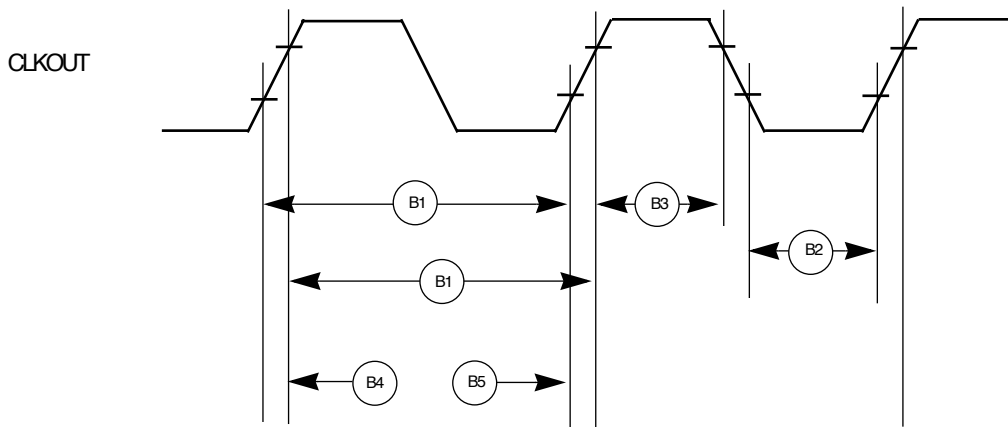
| NUM  | CHARACTERISTIC   | 25MHz |     | 40MHz |     | 50MHz |     | UNIT |
|------|--|-------|-----|-------|-----|-------|-----|------|
|      |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| B31a | CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM, EBDF = 0 | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B31b | CLKOUT Rising Edge to $\overline{CS}$ valid as requested by CST2 in the corresponding word of the UPM            | 1.5   | 10  | 1.5   | 8   | 1.5   | 8   | ns   |
| B31c | CLKOUT Rising Edge to $\overline{CS}$ valid as requested by CST3 in the corresponding word of the UPM            | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B31d | CLKOUT Falling Edge to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM, EBDF = 1 | 10    | 25  | 5     | 16  | 5     | 16  | ns   |
| B32  | CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST4 in the corresponding word of the UPM           | 1.5   | 10  | 1.5   | 8   | 1.5   | 8   | ns   |
| B32a | CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM, EBDF = 0 | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B32b | CLKOUT Rising Edge to $\overline{BS}$ valid as requested by BST2 in the corresponding word of the UPM            | 1.5   | 10  | 1.5   | 8   | 1.5   | 8   | ns   |
| B32c | CLKOUT Rising Edge to $\overline{BS}$ valid as requested by BST3 in the corresponding word of the UPM            | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B32d | CLKOUT Falling Edge to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM, EBDF = 1 | 10    | 25  | 5     | 16  | 5     | 16  | ns   |
| B33  | CLKOUT Falling Edge to $\overline{GPL}$ valid as requested by GxT4 in the corresponding word of the UPM          | 1.5   | 10  | 1.5   | 8   | 1.5   | 8   | ns   |
| B33a | CLKOUT Rising Edge to $\overline{GPL}$ valid as requested by GxT3 in the corresponding word of the UPM           | 10    | 20  | 5     | 13  | 5     | 13  | ns   |
| B34  | A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST4 in the corresponding word of the UPM           | 8     | —   | 3     | —   | 3     | —   | ns   |
| B34a | A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST1 in the corresponding word of the UPM           | 18    | —   | 8     | —   | 8     | —   | ns   |
| B34b | A(6:31) and D(0:31) to $\overline{CS}$ valid as requested by CST2 in the corresponding word of the UPM           | 28    | —   | 13    | —   | 13    | —   | ns   |
| B35  | A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST4 in the corresponding word of the UPM           | 8     | —   | 3     | —   | 3     | —   | ns   |
| B35a | A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST1 in the corresponding word of the UPM           | 18    | —   | 8     | —   | 8     | —   | ns   |
| B35b | A(6:31) and D(0:31) to $\overline{BS}$ valid as requested by BST2 in the corresponding word of the UPM           | 28    | —   | 13    | —   | 13    | —   | ns   |
| B36  | A(6:31) and D(0:31) to $\overline{GPL}$ valid as requested by GxT4 in the corresponding word of the UPM          | 8     | —   | 3     | —   | 3     | —   | ns   |
| B37  | UPWAIT Valid to CLKOUT Falling Edge  | 6     | —   | 6     | —   | 6     | —   | ns   |
| B38  | CLKOUT Falling Edge to UPWAIT Valid  | 1     | —   | 1     | —   | 1     | —   | ns   |
| B39  | $\overline{AS}$ Valid to CLKOUT Rising Edge  | 9     | —   | 7     | —   | 7     | —   | ns   |

**Table 1. Bus Operation Timing (Continued)**

| NUM | CHARACTERISTIC  | 25MHz |     | 40MHz |     | 50MHz |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| B40 | A(6:31), TSIZ(0:1), RD $\overline{WR}$ , $\overline{BURST}$ , Valid to CLKOUT Rising Edge | 9     | —   | 7     | —   | 7     | —   | ns   |
| B41 | $\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)                                  | 9     | —   | 7     | —   | 7     | —   | ns   |
| B42 | CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time)                                   | 2     | —   | 2     | —   | 2     | —   | ns   |
| B43 | $\overline{AS}$ Negation to Memory Controller Signals Negation                            | —     | 13  | —     | 13  | —     | 13  | ns   |

NOTES:

1. The timing for  $\overline{BR}$  output is relevant when the MPC823 is selected to work with the external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the MPC823 is selected to work with the internal bus arbiter.
2. The setup times required for  $\overline{TA}$ ,  $\overline{TEA}$  and  $\overline{BI}$  are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drive them).
3. The timing required for  $\overline{BR}$  input is relevant when the MPC823 is selected to work with the internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC823 is selected to work with the external bus arbiter.
4. The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.
5. The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only under control of the UPM in the memory controller.
6. The timing B30 refers to  $\overline{CS}$  when ACS = '00' and to  $\overline{WE}(0:3)$  when CSNT = '0'.
7. The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.
8. The  $\overline{AS}$  signal is considered asynchronous to the CLKOUT signal.



**Figure 1. External Clock Timing Diagram**

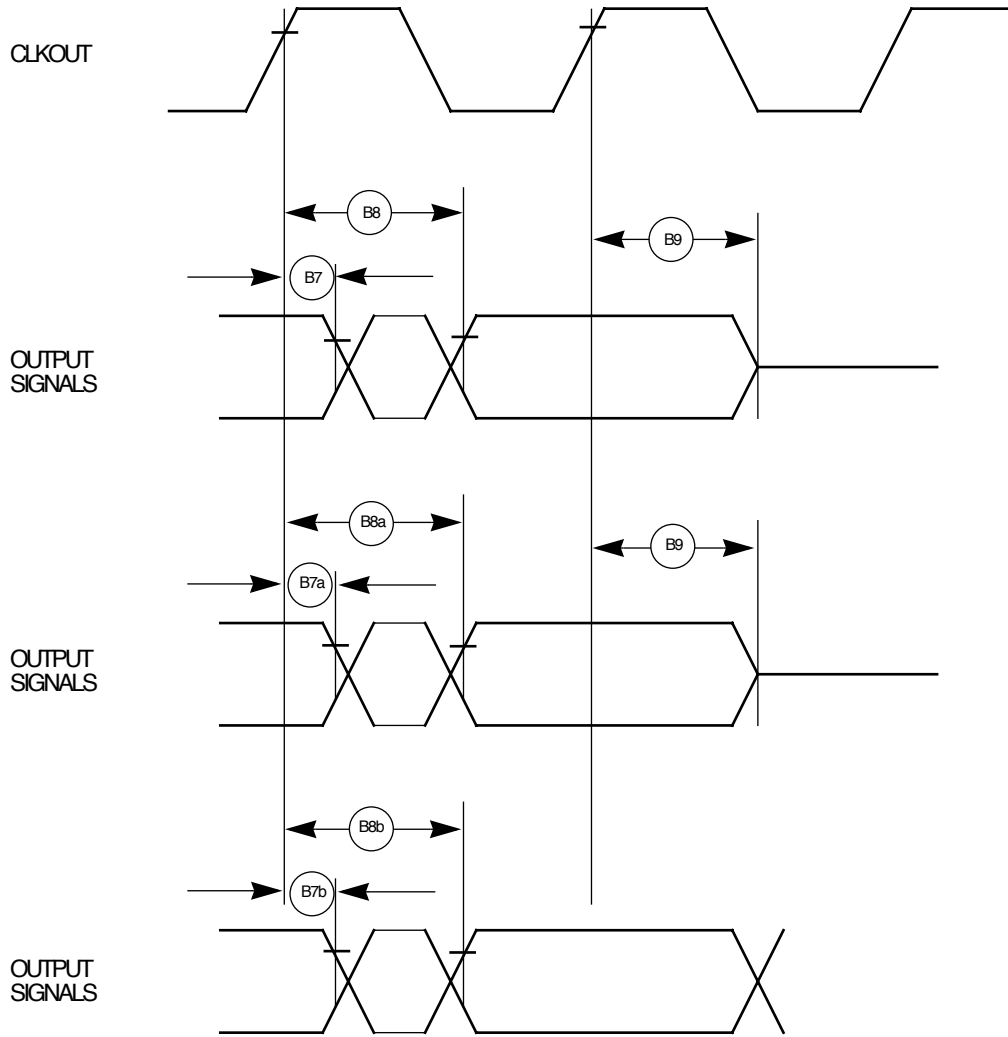


Figure 2. Synchronous Output Signals Timing Diagram

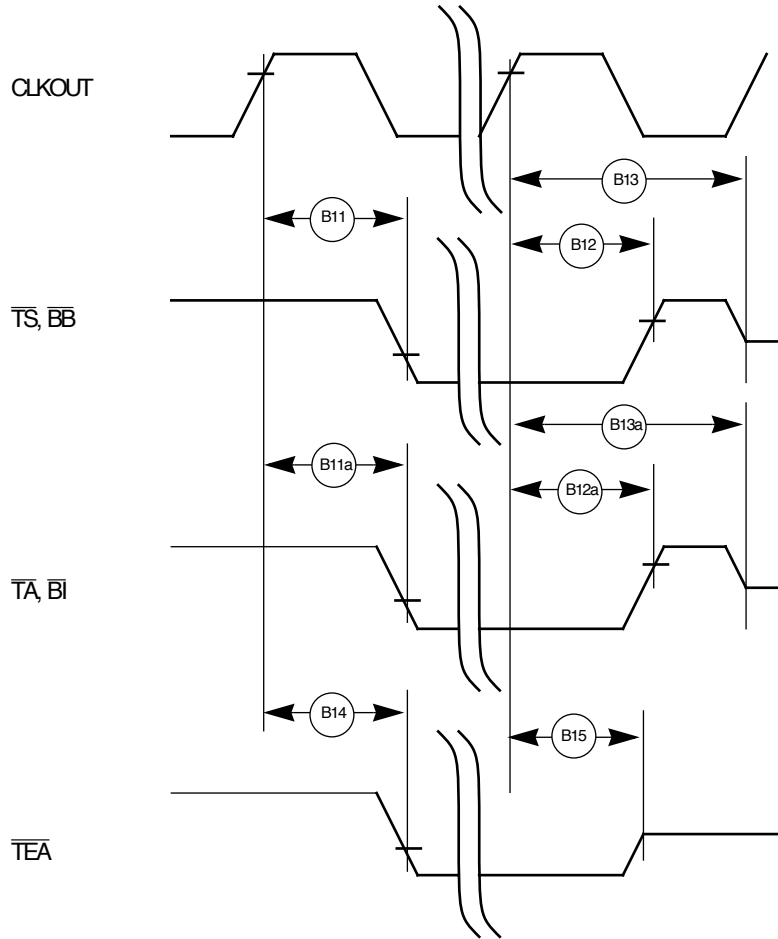


Figure 3. Synchronous Active Pull-Up and Open-Drain Outputs Signals Timing Diagram

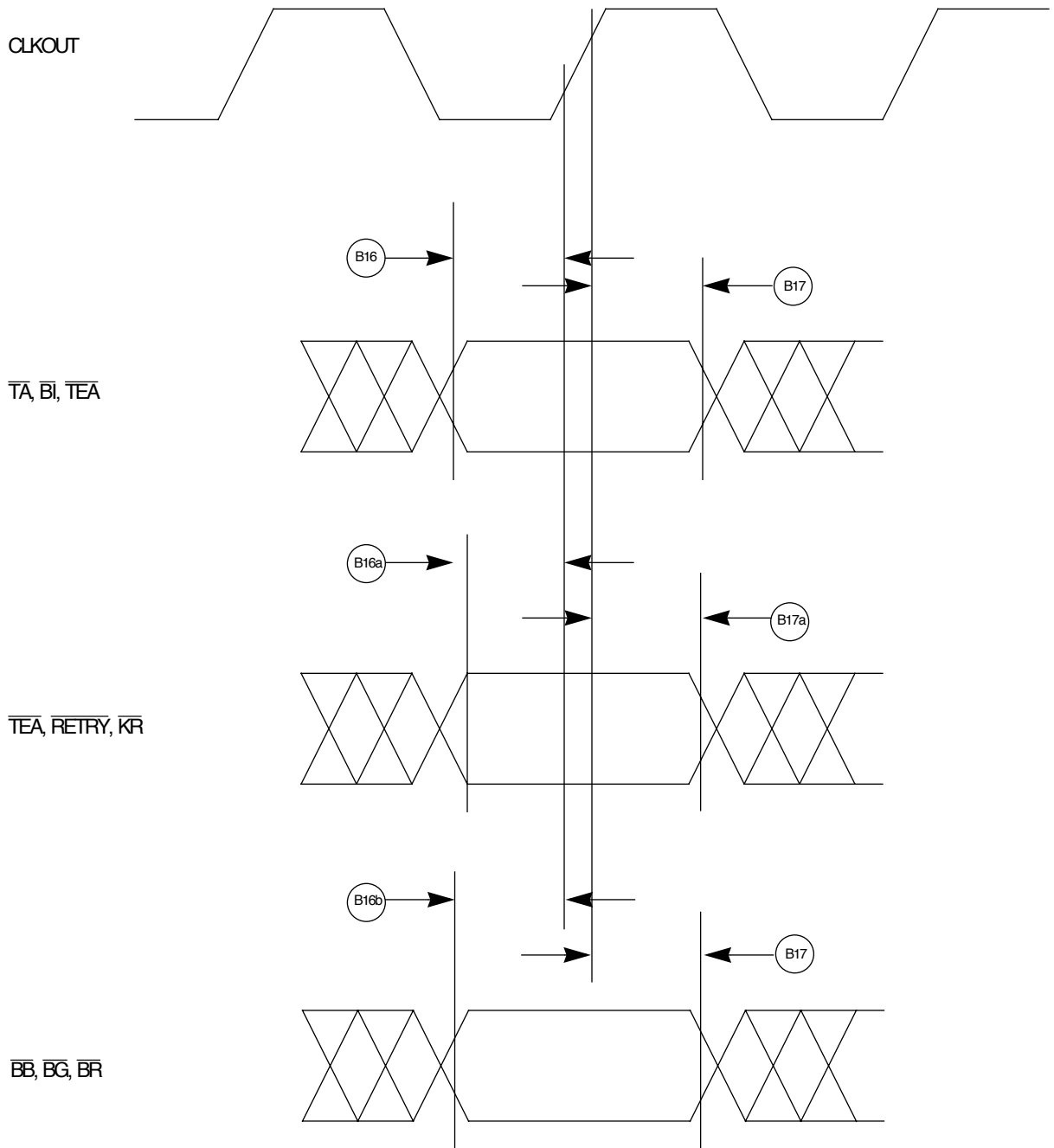
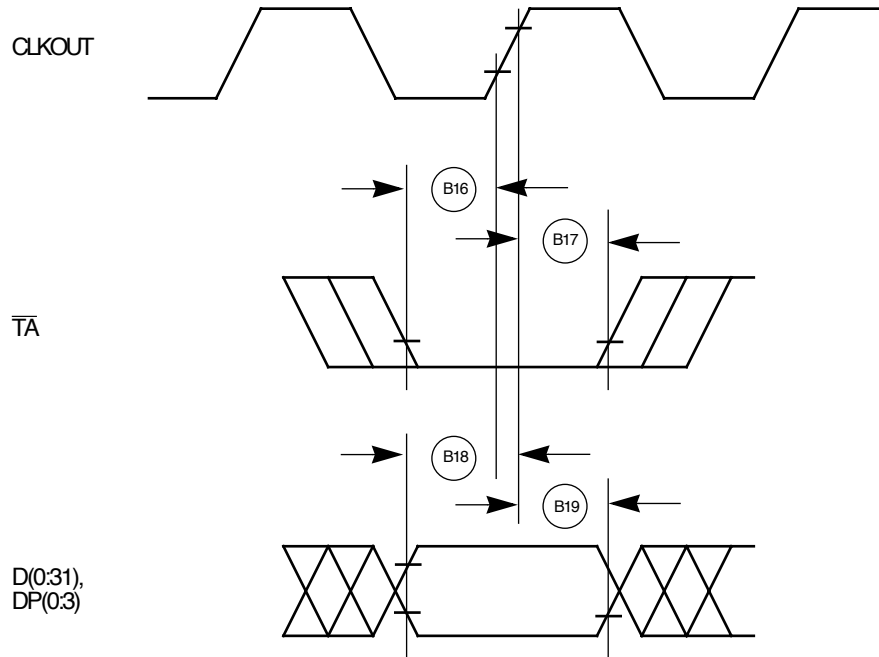
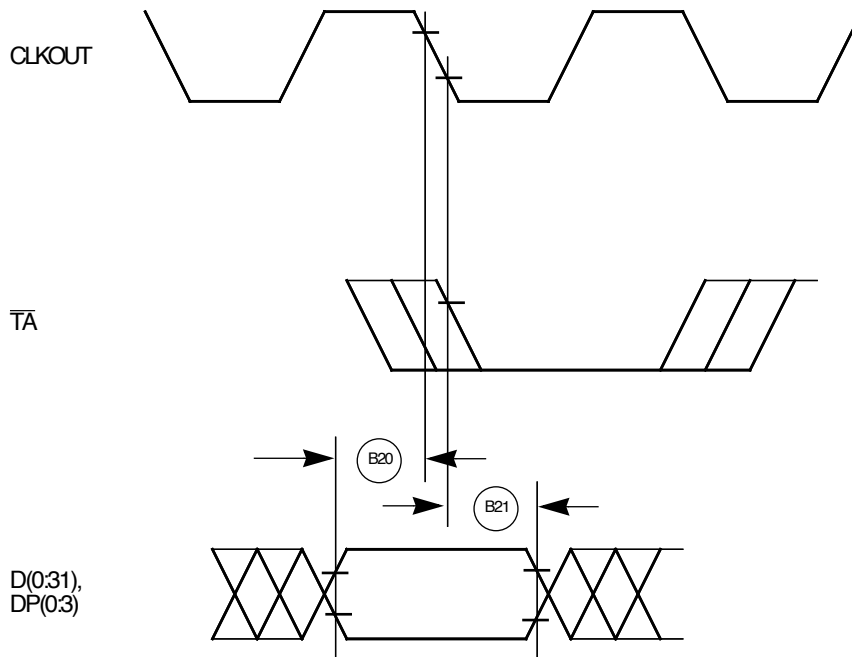


Figure 4. Synchronous Input Signals Timing Diagram



**Figure 5. Input Data In Normal Case Timing Diagram**



**Figure 6. Input Data When Controlled by the UPM Timing Diagram**

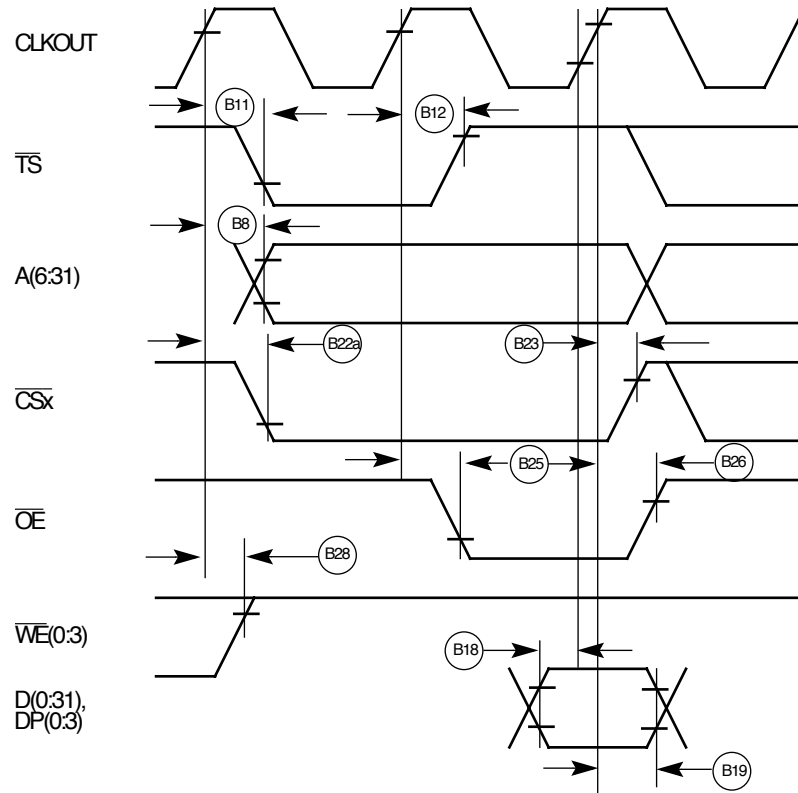


Figure 7. External Bus Read Timing Diagram (GPCM Controlled—ACS = '00')

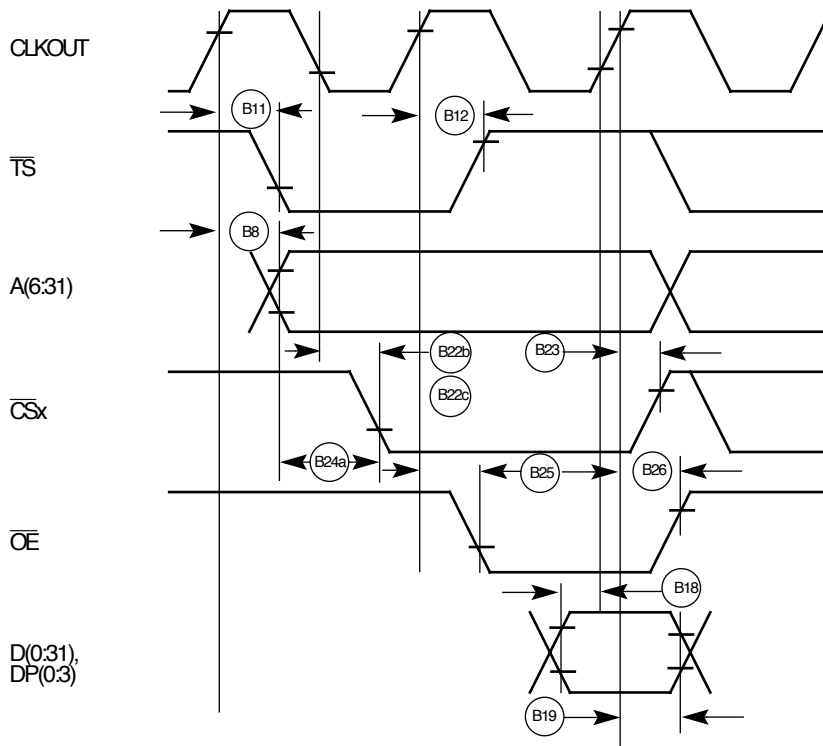


Figure 8. External Bus Read Timing Diagram (GPCM Controlled—TRLX = '0', ACS = '10')

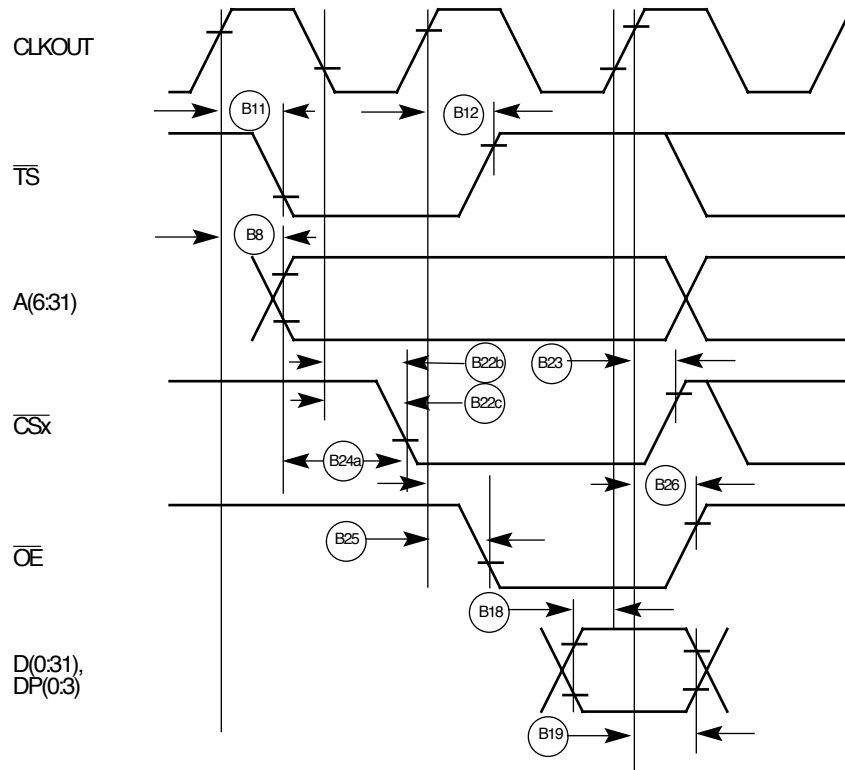
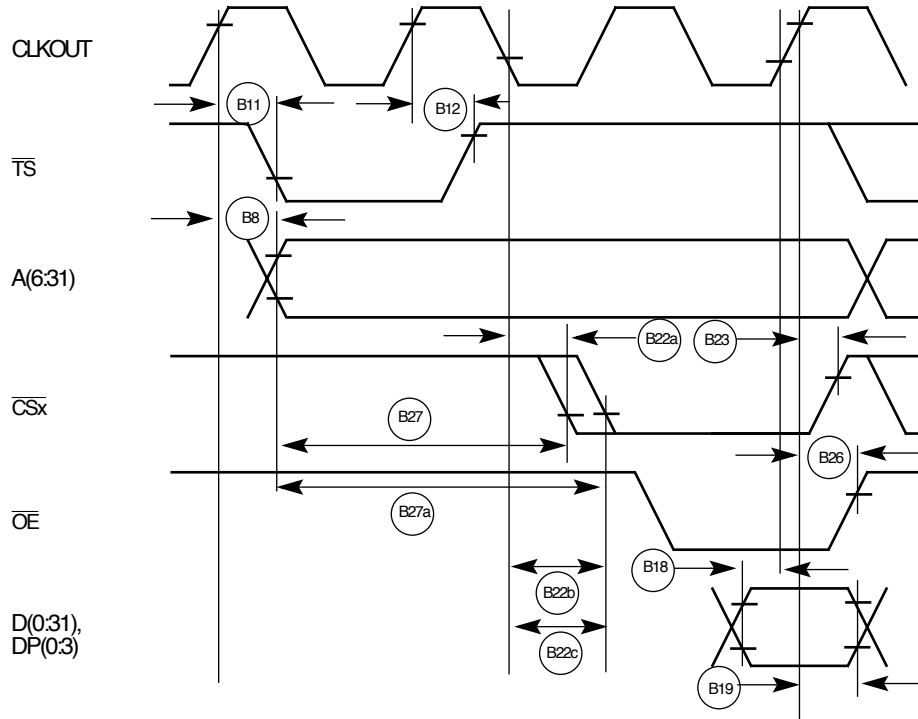


Figure 9. External Bus Read Timing Diagram  
(GPCM Controlled—TRLX = '0', ACS = '11')





**Figure 10. External Bus Read Timing Diagram**  
 (GPCM Controlled—TRLX = '1', ACS = '10', ACS = '11')

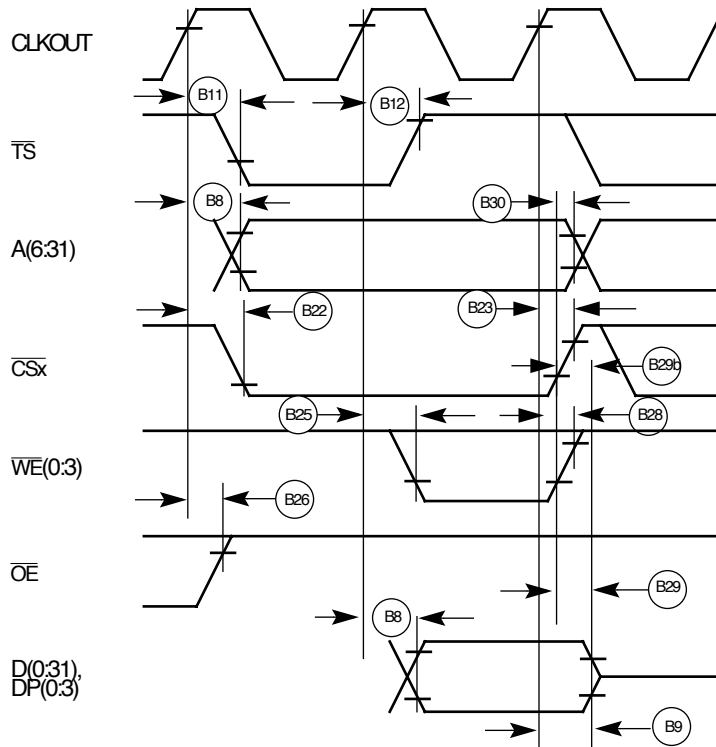


Figure 11. External Bus Write Timing Diagram  
(GPCM Controlled—TRLX = '0', CSNT = '0')

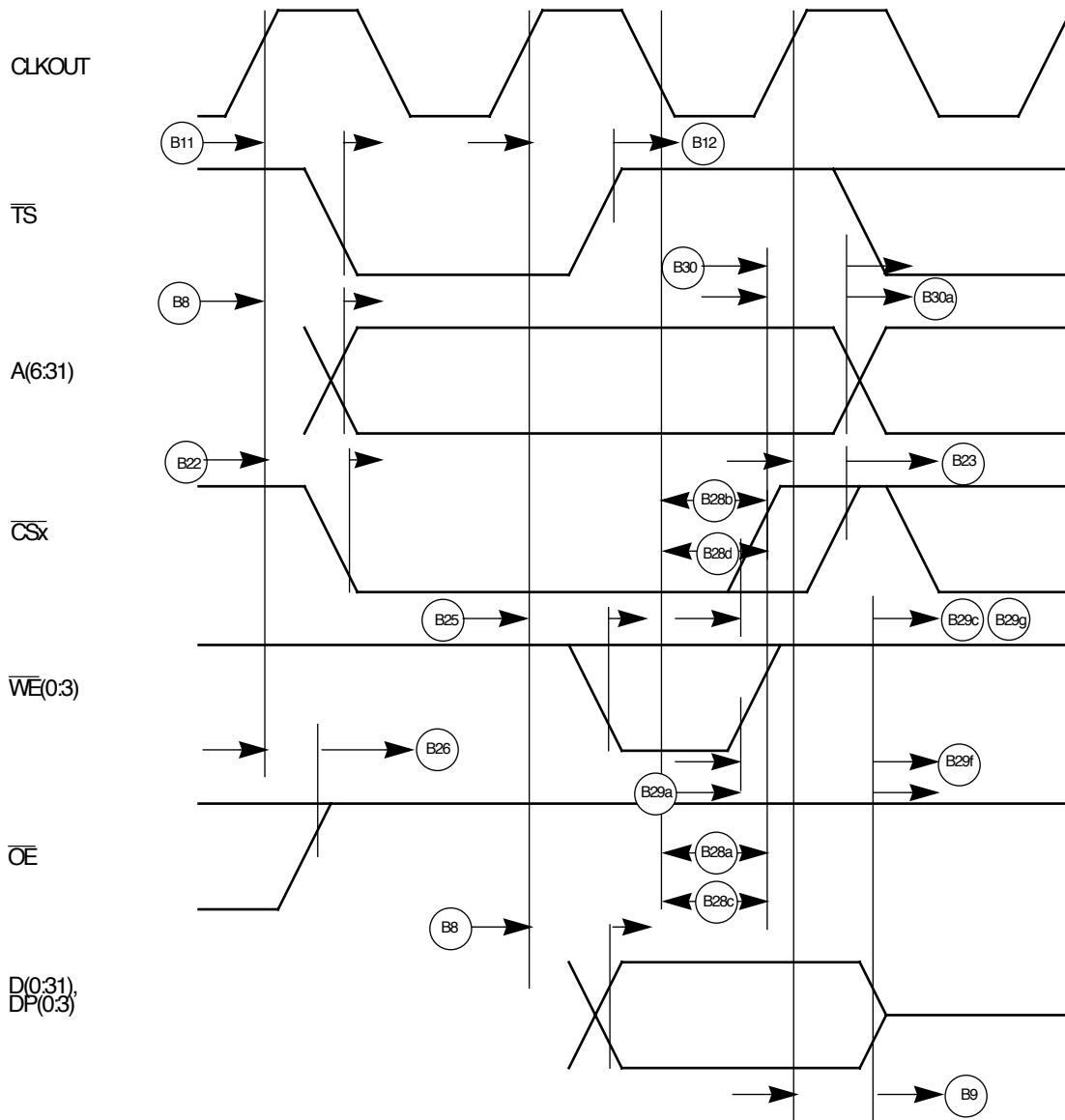


Figure 12. External Bus Write Timing Diagram  
(GPCM Controlled-TRLX = '0', CSNT = '1')

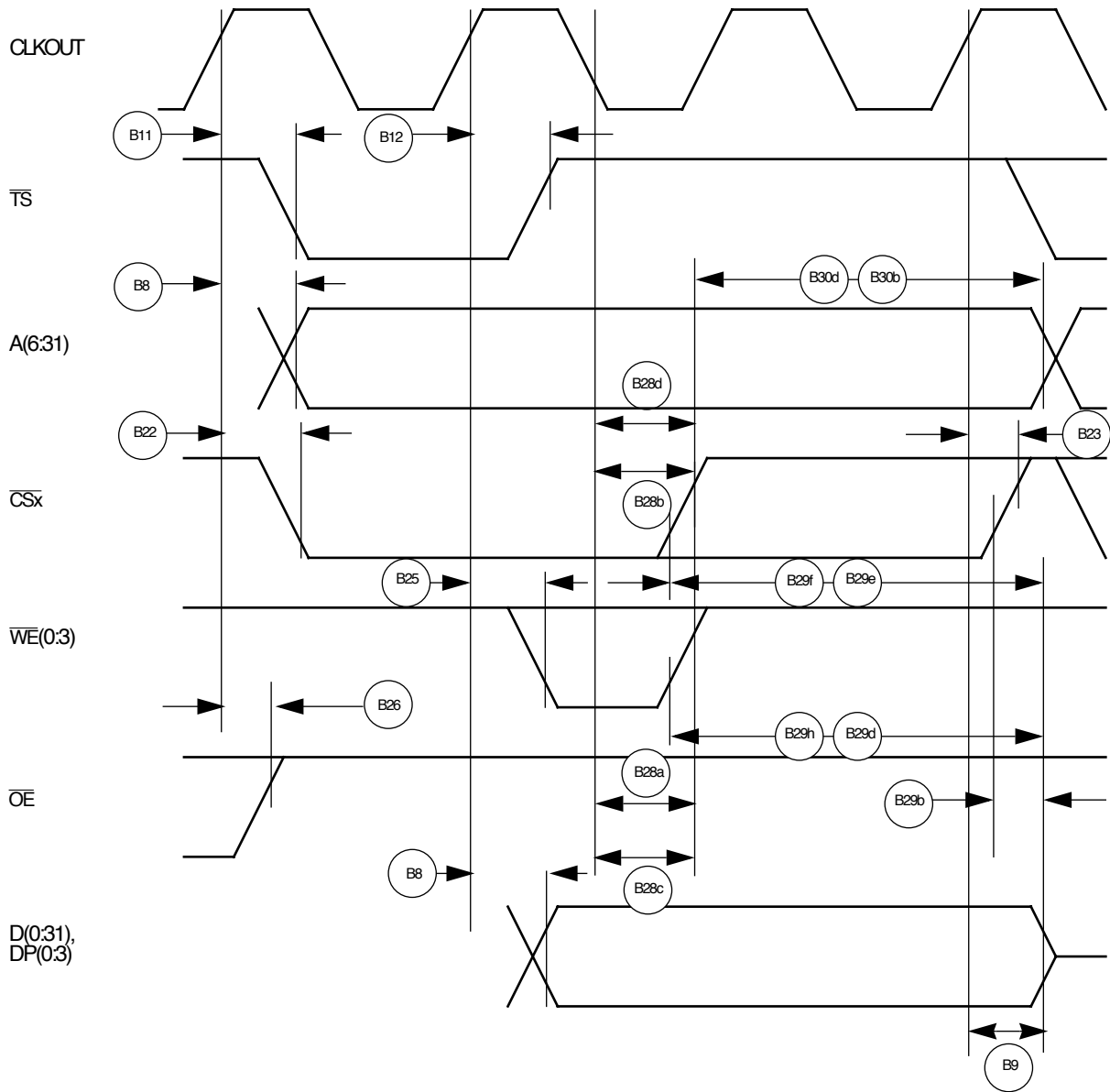


Figure 13. External Bus Write Timing Diagram  
(GPCM Controlled—TRLX = '1', CSNT = '1')

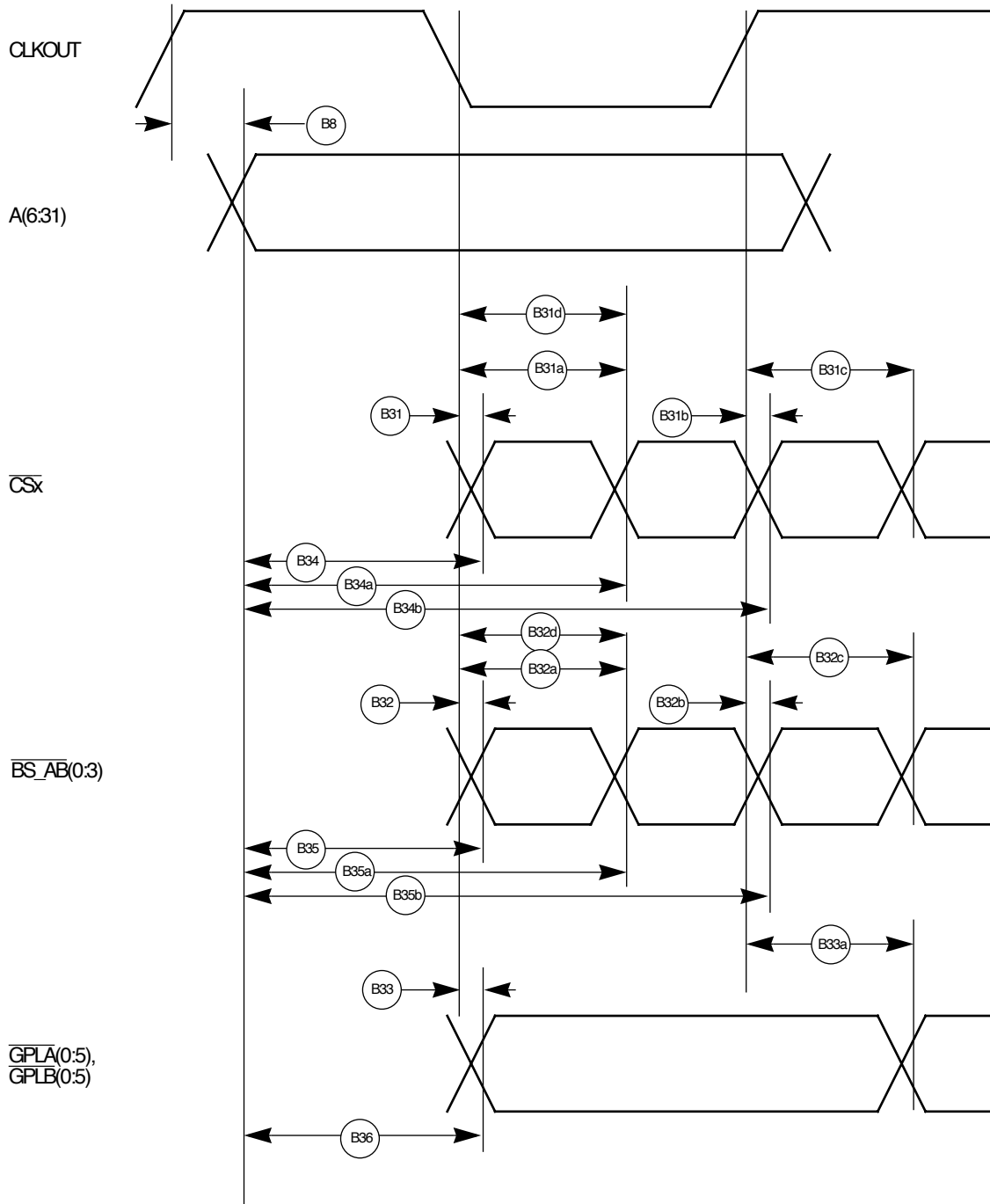


Figure 14. External Bus Timing Diagram (UPM-Controlled Signals)

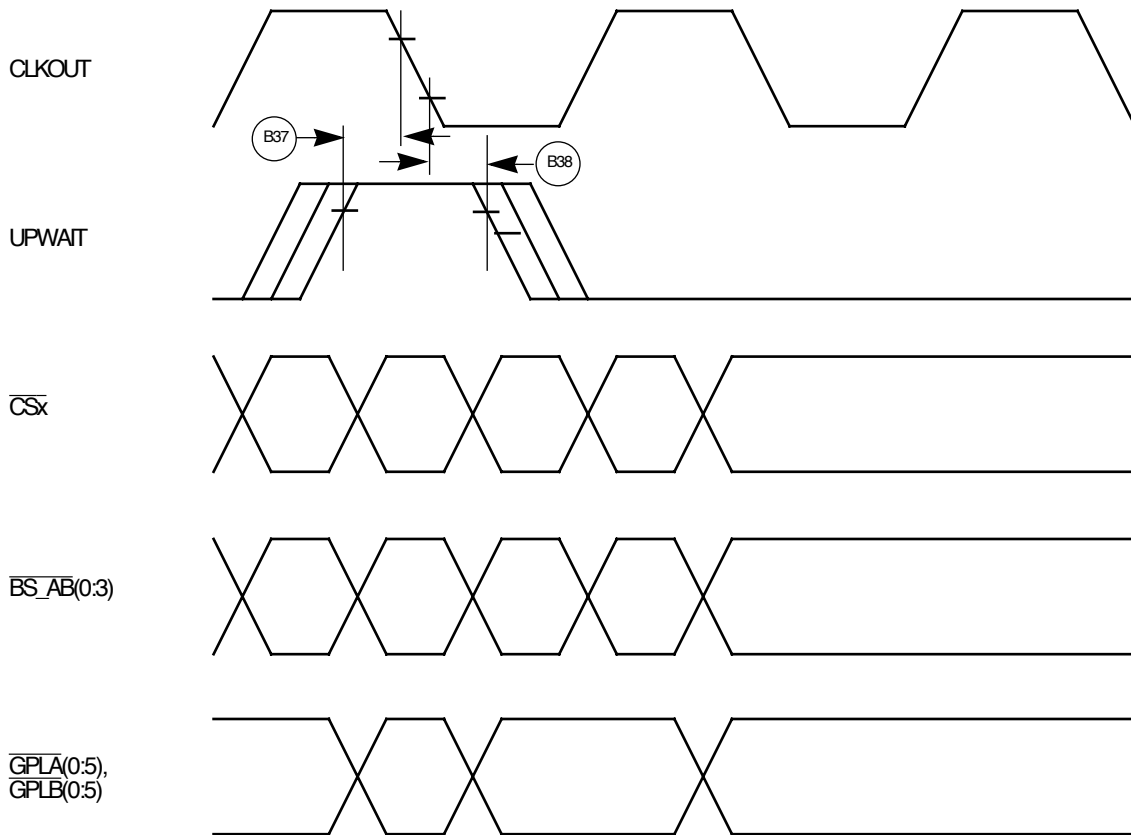


Figure 15. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing Diagram

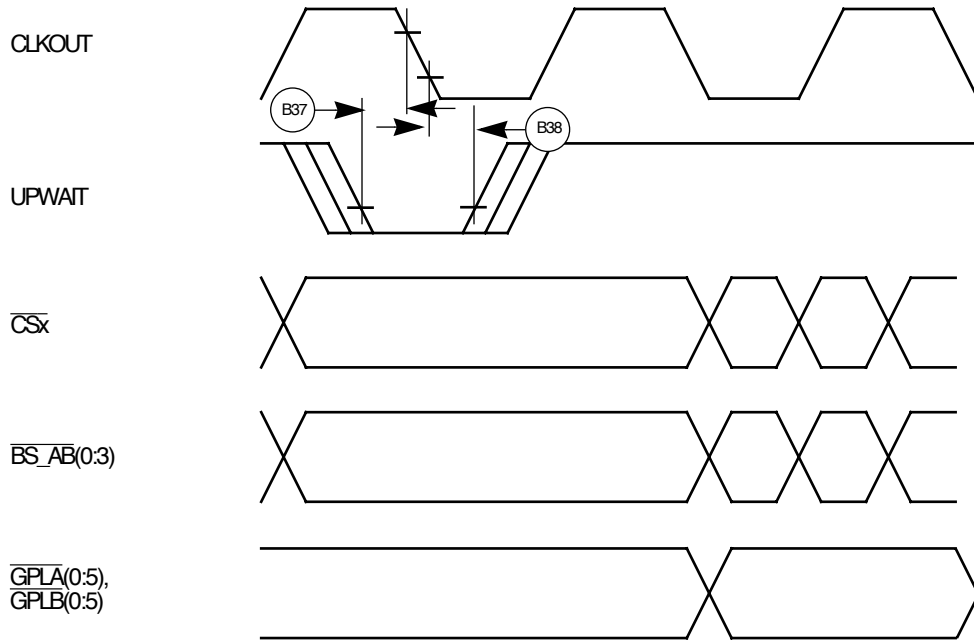


Figure 16. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing Diagram

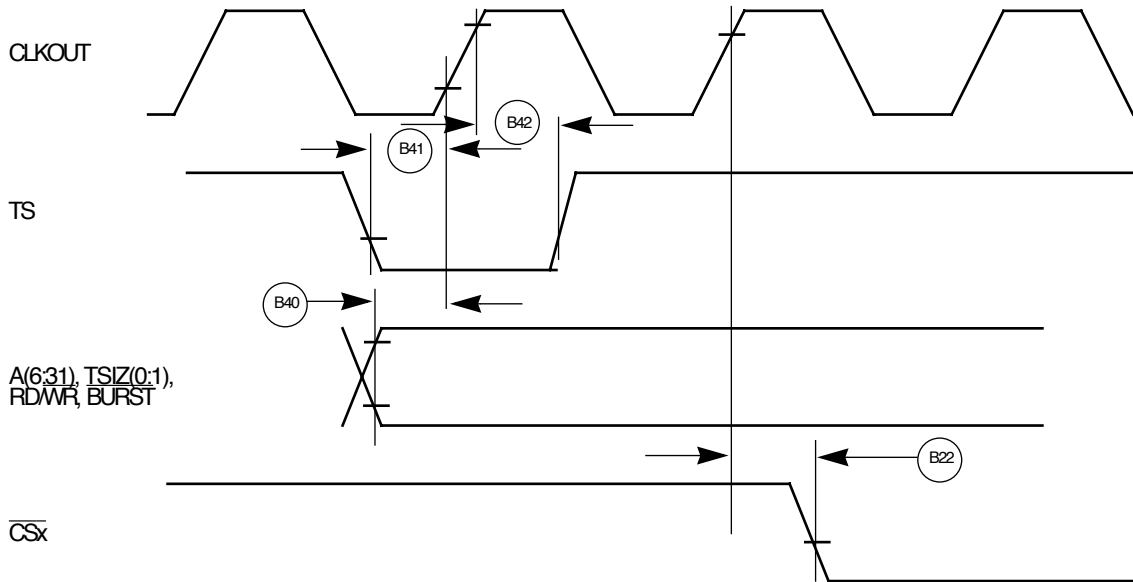


Figure 17. Synchronous External Master Access Timing Diagram (GPCM Handled—ACS = '00')

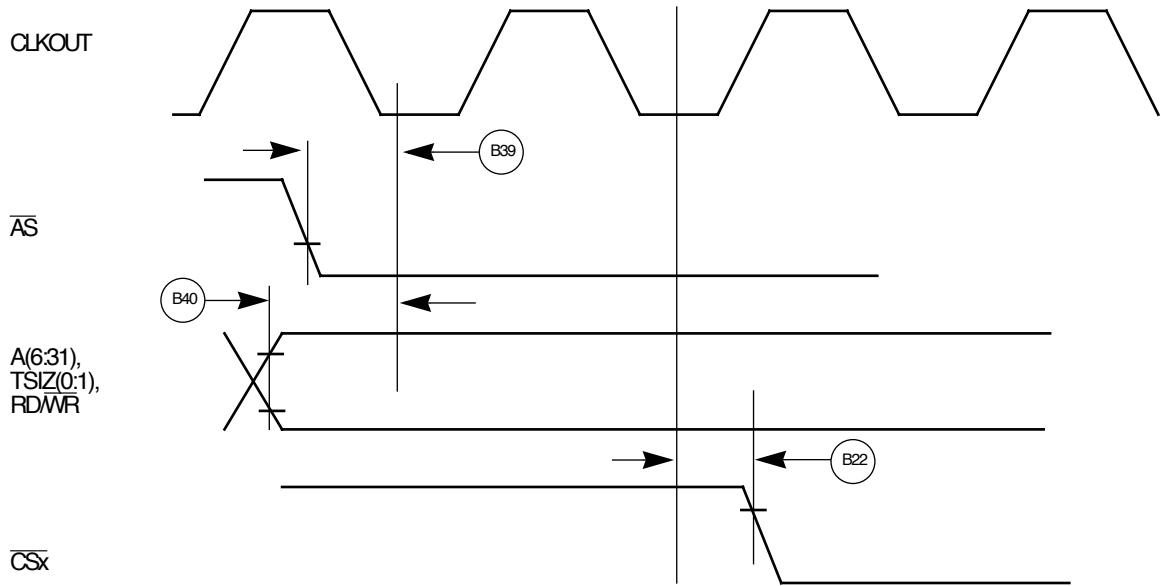


Figure 18. Asynchronous External Master Memory Access Timing Diagram (GPCM Controlled—ACS = '00')

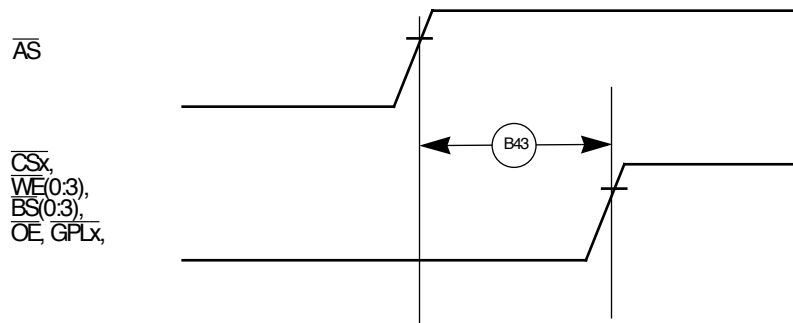


Figure 19. Asynchronous External Master Timing Diagram (Control Signals Negation Time)



Table 2. Interrupt Timing

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| I39 | $\overline{\text{IRQx}}$ valid to CLKOUT rising edge (setup time) | 6     | —   | 6/6   | —   | 6/6   | —   | ns   |
| I40 | $\overline{\text{IRQx}}$ hold time after CLKOUT                   | 2     | —   | 2/2   | —   | 2/2   | —   | ns   |
| I41 | $\overline{\text{IRQx}}$ pulse width low                          | 3     | —   | 3/3   | —   | 3/3   | —   | ns   |
| I42 | $\overline{\text{IRQx}}$ pulse width high                         | 3     | —   | 3/3   | —   | 3/3   | —   | ns   |
| I43 | $\overline{\text{IRQx}}$ edge to edge time                        | 160   | —   | 80/80 | —   | 80/80 | —   | ns   |

NOTES:

1. The timings I39 and I40 describe the testing conditions under which the  $\overline{\text{IRQ}}$  lines are tested when defined as level sensitive. The  $\overline{\text{IRQ}}$  lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
2. The timings I41 and I42 are specified to allow the correct function of the  $\overline{\text{IRQ}}$  lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC823 can support.

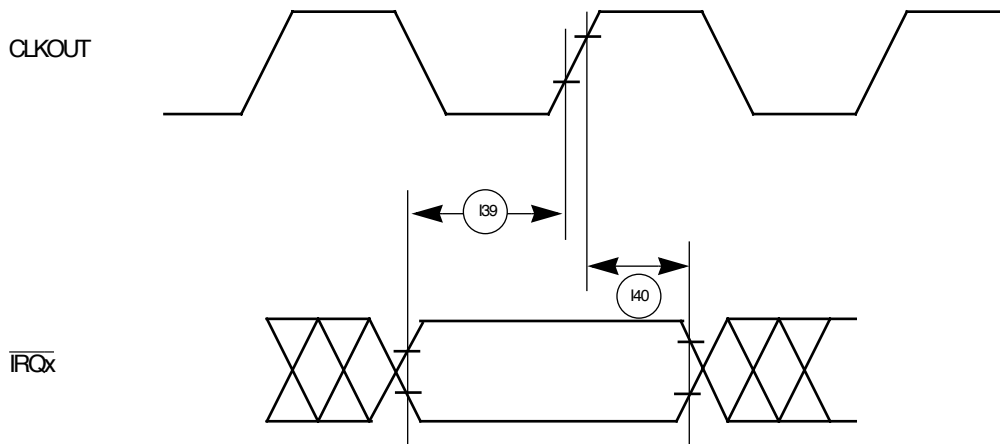


Figure 20. Interrupt Detection Timing Diagram for External Level-Sensitive Lines

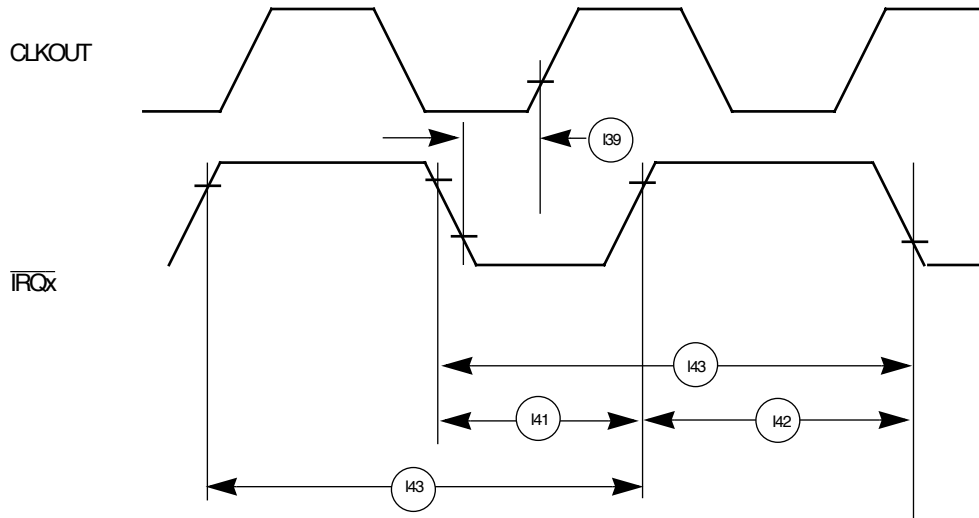


Figure 21. Interrupt Detection Timing Diagram for External Edge-Sensitive Lines

Table 3. PCMCIA Timing

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| P44 | A(6:31), $\overline{REG}$ valid to PCMCIA strobe asserted   | 28    | —   | 13    | —   | 13    | —   | ns   |
| P45 | A(6:31), $\overline{REG}$ valid to ALE negation   | 38    | —   | 18    | —   | 18    | —   | ns   |
| P46 | CLKOUT to $\overline{REG}$ valid  | 10    | 19  | 5     | 13  | 5     | 13  | ns   |
| P47 | CLKOUT to $\overline{REG}$ invalid  | 11    | —   | 6     | —   | 6     | —   | ns   |
| P48 | CLKOUT to $\overline{CE1}$ , $\overline{CE2}$ asserted  | 10    | 19  | 5     | 13  | 5     | 13  | ns   |
| P49 | CLKOUT to $\overline{CE1}$ , $\overline{CE2}$ negated   | 10    | 19  | 5     | 13  | 5     | 13  | ns   |
| P50 | CLKOUT to $\overline{PCOE}$ , $\overline{IORD}$ , $\overline{PCWE}$ , $\overline{IOWR}$ assert time | —     | 12  | —     | 11  | —     | 11  | ns   |
| P51 | CLKOUT to $\overline{PCOE}$ , $\overline{IORD}$ , $\overline{PCWE}$ , $\overline{IOWR}$ negate time | 3     | 12  | 2     | 11  | 2     | 11  | ns   |
| P52 | CLKOUT to ALE assert time   | 10    | 19  | 5     | 13  | 5     | 13  | ns   |
| P53 | CLKOUT to ALE negate time   | —     | 19  | —     | 13  | —     | 13  | ns   |
| P54 | $\overline{PCWE}$ , $\overline{IOWR}$ negated to D(0:31) invalid                                    | 8     | —   | 3     | —   | 3     | —   | ns   |
| P55 | $\overline{WAIT\_B}$ valid to CLKOUT rising edge  | 8     | —   | 8     | —   | 8     | —   | ns   |
| P56 | CLKOUT rising edge to $\overline{WAIT\_B}$ invalid  | 2     | —   | 2     | —   | 2     | —   | ns   |

NOTES:

1. PSST = 1. Otherwise, add PSST times cycle time.
2. PSHT = 0. Otherwise, add PSHT times cycle time.
3. These synchronous timings define when the  $\overline{WAIT\_B}$  signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The  $\overline{WAIT\_B}$  assertion will be effective only if it is detected two cycles before the PSL timer expiration.

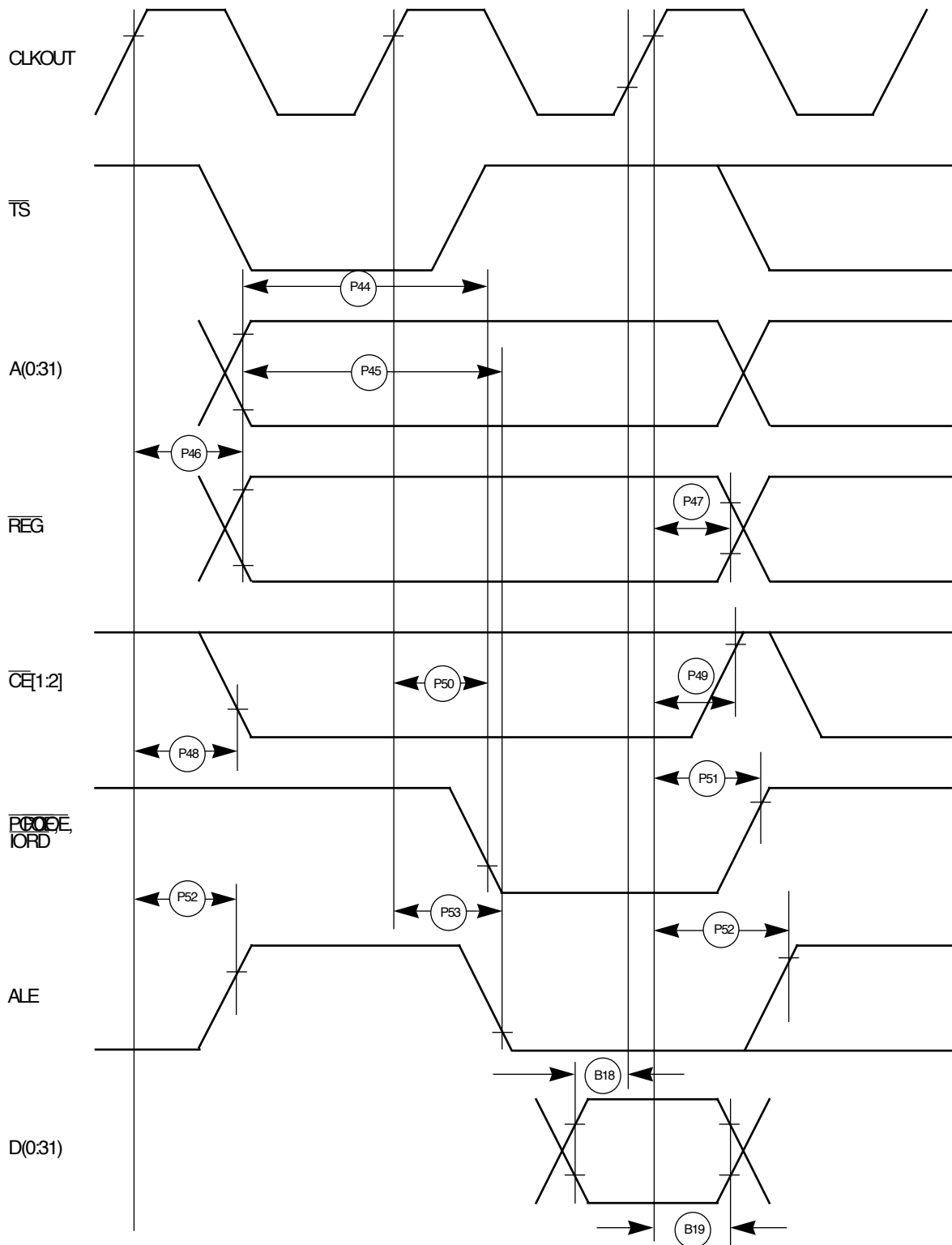


Figure 22. PCMCIA Access Cycles Timing Diagram (External Bus Read)

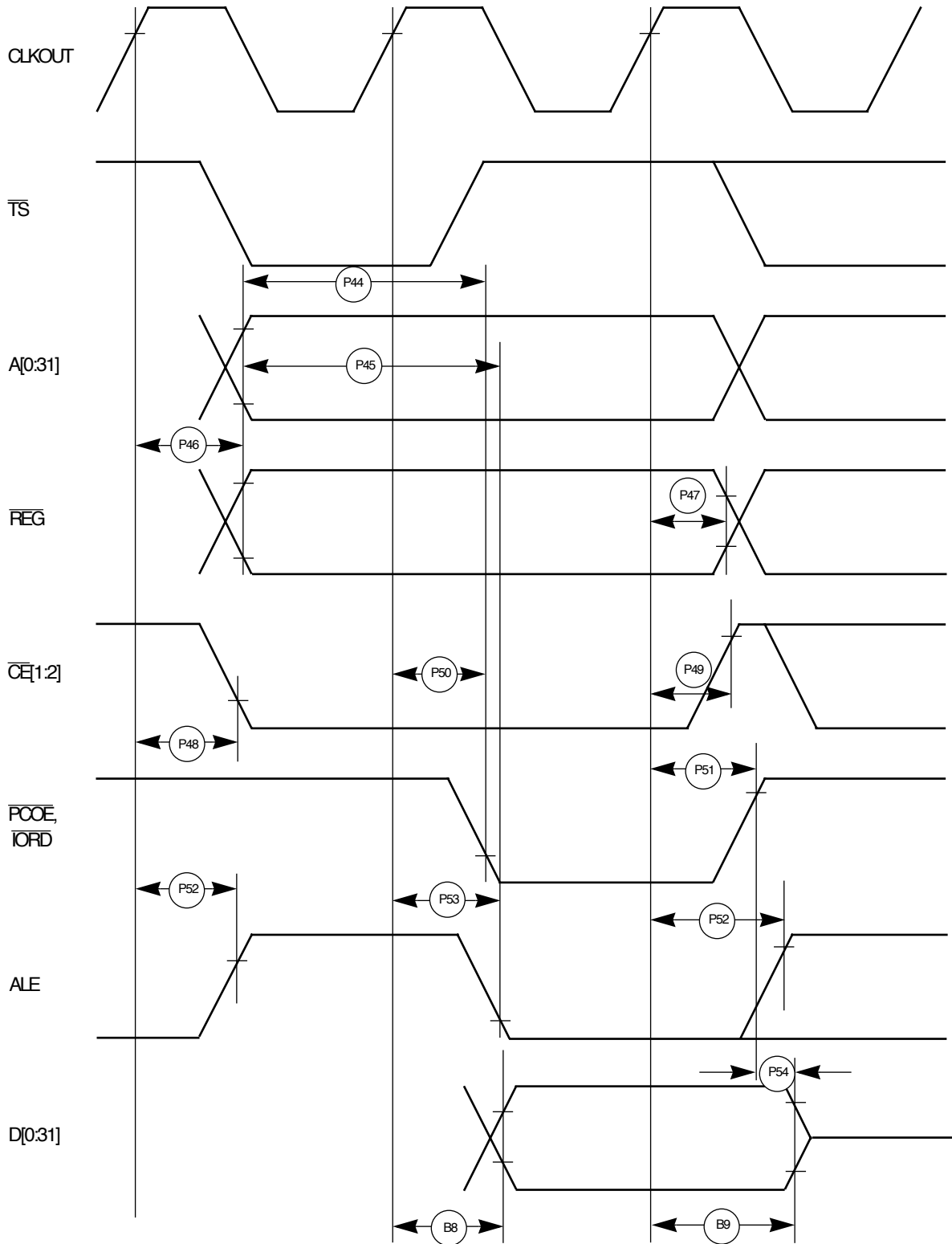


Figure 23. PCMCIA Access Cycles Timing Diagram (External Bus Write)

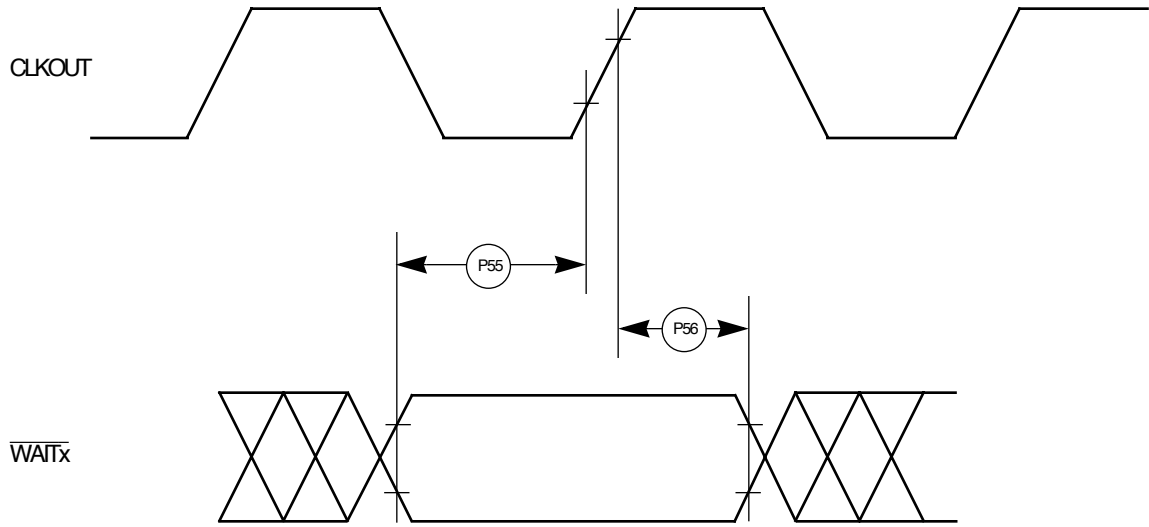


Figure 24. PCMCIA Wait Signals Detection Timing Diagram

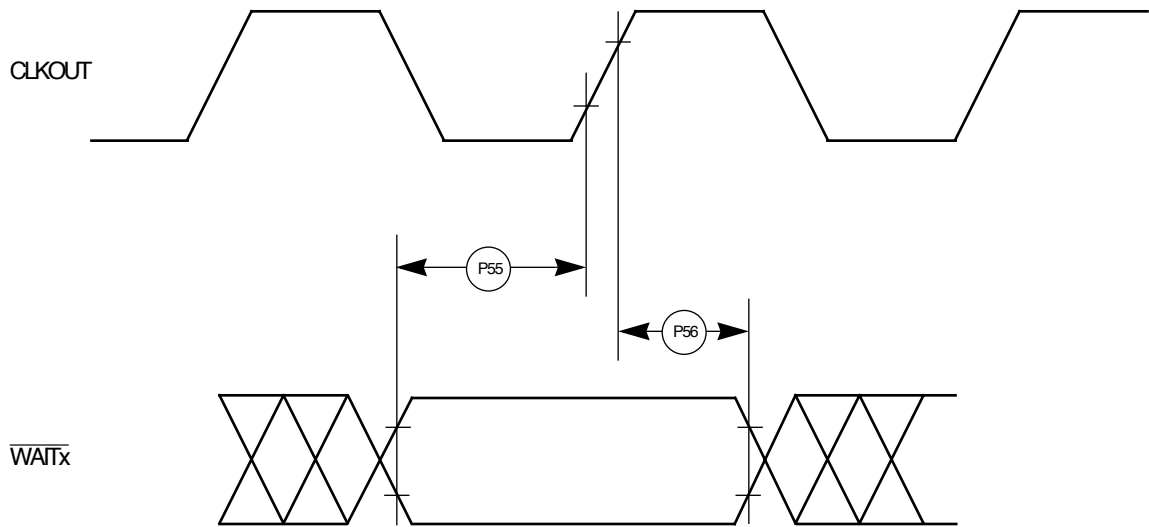


Figure 25. PCMCIA Wait Signals Detection Timing Diagram

Table 4. PCMCIA Port Timing

| NUM | CHARACTERISTIC                      | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|-------------------------------------|-------|-----|-------|-----|-------|-----|------|
|     |                                     | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| P57 | CLKOUT to OPx Valid                 | —     | 25  | —     | 19  | —     | 19  | ns   |
| P58 | HRESET negated to OPx drive         | 30    | —   | 18    | —   | 18    | —   | ns   |
| P59 | IP_Bx valid to CLKOUT Rising Edge   | 6     | —   | 5     | —   | 5     | —   | ns   |
| P60 | CLKOUT Rising Edge to IP_Bx invalid | 2     | —   | 1     | —   | 1     | —   | ns   |

NOTE: \*OP2 and OP3 only.

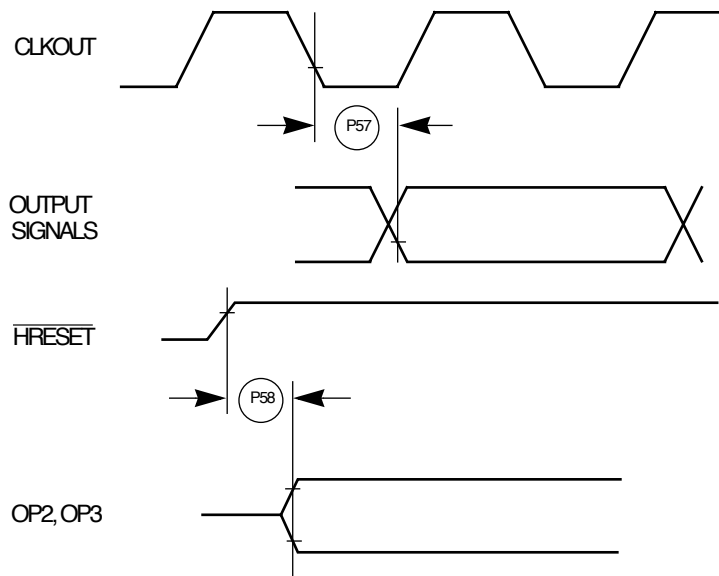


Figure 26. PCMCIA Output Port Timing Diagram

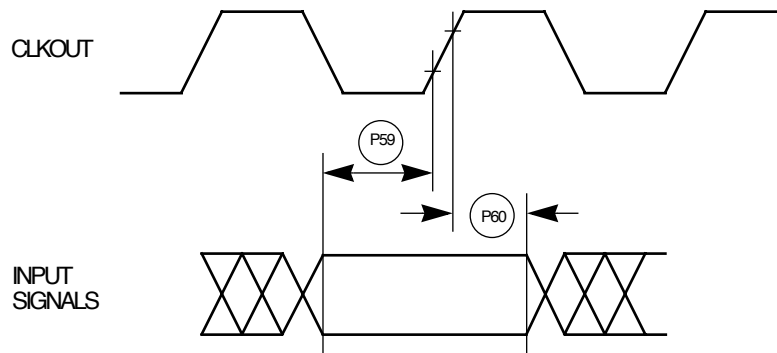


Figure 27. PCMCIA Input Port Timing Diagram

Table 5. Debug Port Timing

| NUM | CHARACTERISTIC              | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|-----------------------------|-------|-----|-------|-----|-------|-----|------|
|     |                             | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| D61 | DSCK cycle time             | 120   | —   | 60    | —   | 60    | —   | ns   |
| D62 | DSCK clock pulse width      | 50    | —   | 25    | —   | 25    | —   | ns   |
| D63 | DSCK rise and fall times    | 0     | 3   | 0     | 3   | 0     | 3   | ns   |
| D64 | DSDI input data setup time  | 8     | —   | 8     | —   | 8     | —   | ns   |
| D65 | DSDI data hold time         | 5     | —   | 5     | —   | 5     | —   | ns   |
| D66 | DSCK low to DSDO data valid | 0     | 15  | 0     | 15  | 0     | 15  | ns   |
| D67 | DSCK low to DSDO invalid    | 0     | 2   | 0     | 2   | 0     | 2   | ns   |

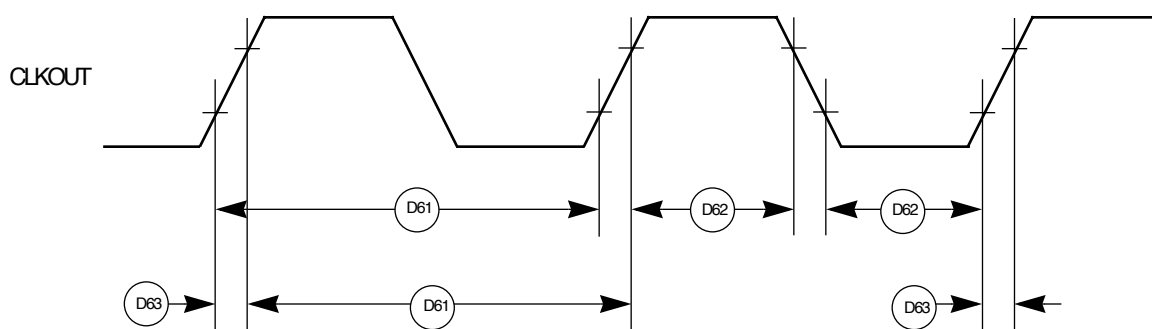


Figure 28. Debug Port Clock Input Timing Diagram



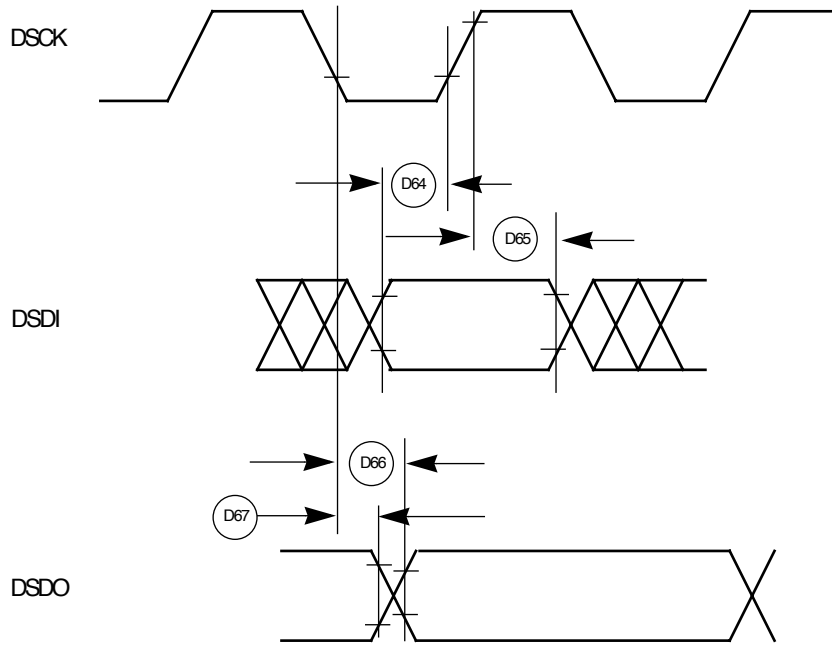


Figure 29. Debug Port Timing Diagram

**Table 6. Reset Timing**

| NUM | CHARACTERISTIC   | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|--|-------|-----|-------|-----|-------|-----|------|
|     |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| R68 | CLKOUT to $\overline{\text{HRESET}}$ high impedance  | —     | 20  | —     | 20  | —     | 20  | ns   |
| R69 | CLKOUT to $\overline{\text{SRESET}}$ high impedance  | —     | 20  | —     | 20  | —     | 20  | ns   |
| R70 | $\overline{\text{RSTCONF}}$ pulse width  | 680   | —   | 425   | —   | 340   | —   | ns   |
| R71 | N/A  |       |     |       |     |       |     |      |
| R72 | Configuration data to $\overline{\text{HRESET}}$ rising edge setup time                                      | 650   | —   | 425   | —   | 350   | —   | ns   |
| R73 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time                                     | 650   | —   | 425   | —   | 350   | —   | ns   |
| R74 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation                                      | 0     | —   | 0     | —   | 0     | —   | ns   |
| R75 | Configuration data hold time after $\overline{\text{HRESET}}$ negation                                       | 0     | —   | 0     | —   | 0     | —   | ns   |
| R76 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive                        | —     | 25  | —     | 25  | —     | 25  | ns   |
| R77 | $\overline{\text{RSTCONF}}$ negated to data out high impedance   | —     | 25  | —     | 25  | —     | 25  | ns   |
| R78 | CLKOUT of last rising edge before chip three-states<br>$\overline{\text{HRESET}}$ to data out high impedance | —     | 25  | —     | 25  | —     | 25  | ns   |
| R79 | DSDI and DSCK setup  | 120   | —   | 75    | —   | 60    | —   | ns   |
| R80 | DSDI and DSCK hold time  | 0     | —   | 0     | —   | 0     | —   | ns   |
| R81 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample                            | 320   | —   | 200   | —   | 160   | —   | ns   |

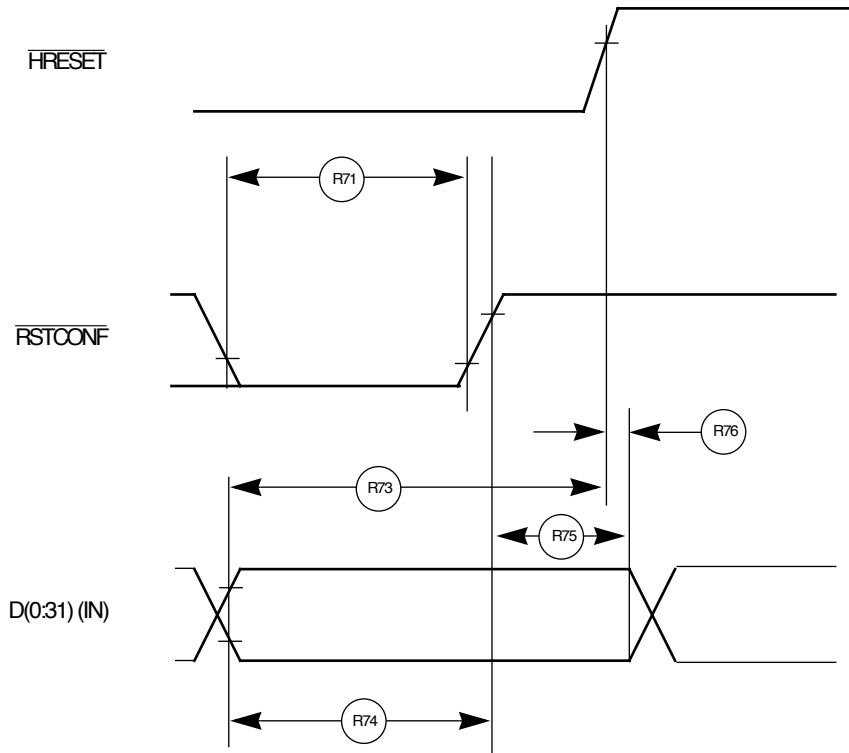


Figure 30. Reset Timing Diagram (Configuration from Data Bus)

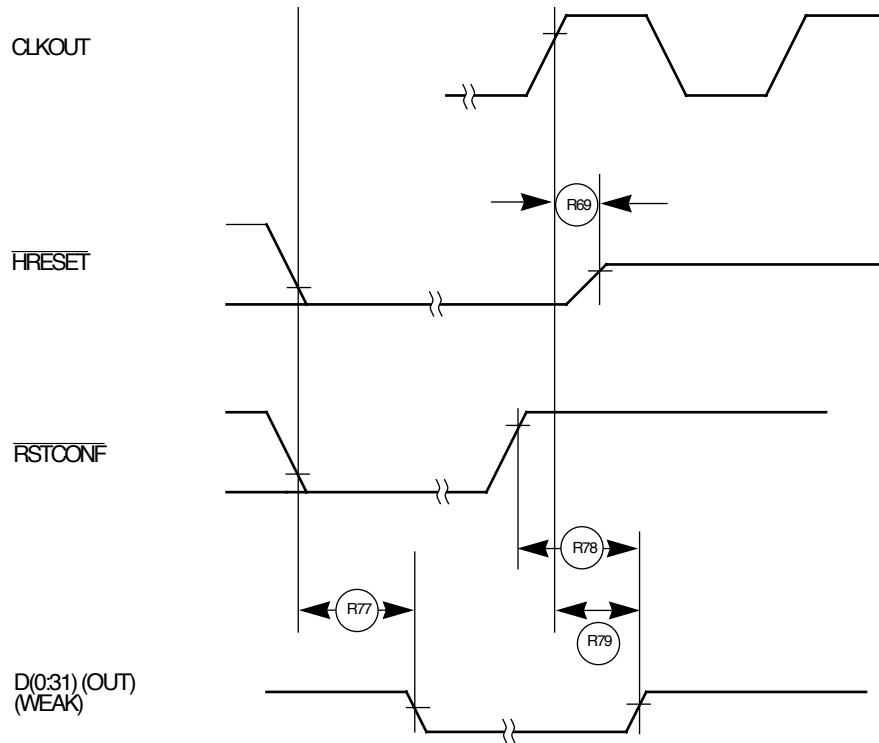


Figure 31. Reset Timing Diagram—MPC823 Data Bus Weak Drive During Configuration

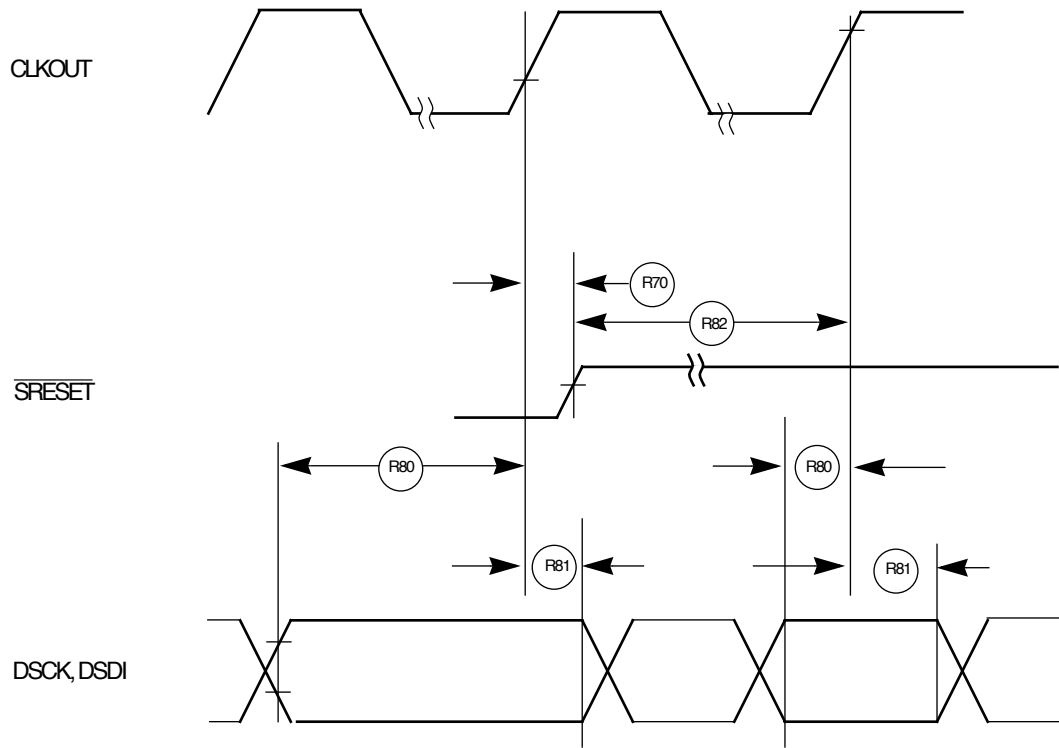


Figure 32. Reset Timing Diagram—Debug Port Configuration

Table 7. JTAG Timing

| NUM | CHARACTERISTIC   | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|--|-------|-----|-------|-----|-------|-----|------|
|     |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| J82 | TCK cycle time   | 100   | —   | 100   | —   | 100   | —   | ns   |
| J83 | TCK clock pulse width measured at 1.5V                 | 40    | —   | 40    | —   | 40    | —   | ns   |
| J84 | TCK rise and fall times                                | 0     | 10  | 0     | 10  | 0     | 10  | ns   |
| J85 | TMS, TDI data setup time                               | 5     | —   | 5     | —   | 5     | —   | ns   |
| J86 | TMS, TDI data hold time                                | 25    | —   | 25    | —   | 25    | —   | ns   |
| J87 | TCK low to TDO data valid                              | —     | 27  | —     | 27  | —     | 27  | ns   |
| J88 | TCK low to TDO data invalid                            | 0     | —   | 0     | —   | 0     | —   | ns   |
| J89 | TCK low to TDO high impedance                          | —     | 20  | —     | 20  | —     | 20  | ns   |
| J90 | $\overline{\text{TRST}}$ assert time                   | 100   | —   | 100   | —   | 100   | —   | ns   |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low         | 40    | —   | 40    | —   | 40    | —   | ns   |
| J92 | TCK falling edge to output valid                       | —     | 50  | —     | 50  | —     | 50  | ns   |
| J93 | TCK falling edge to output valid out of high impedance | —     | 50  | —     | 50  | —     | 50  | ns   |
| J94 | TCK falling edge to output high impedance              | —     | 50  | —     | 50  | —     | 50  | ns   |
| J95 | Boundary scan input valid to TCK rising edge           | 50    | —   | 50    | —   | 50    | —   | ns   |
| J96 | TCK rising edge to boundary scan input invalid         | 50    | —   | 50    | —   | 50    | —   | ns   |

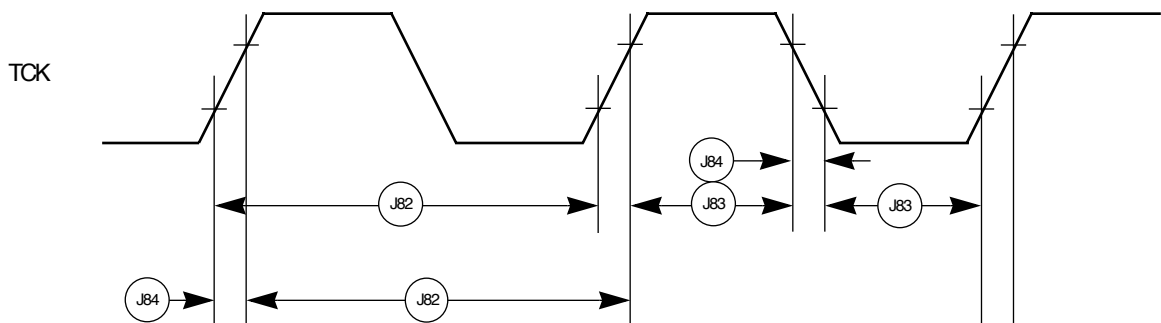
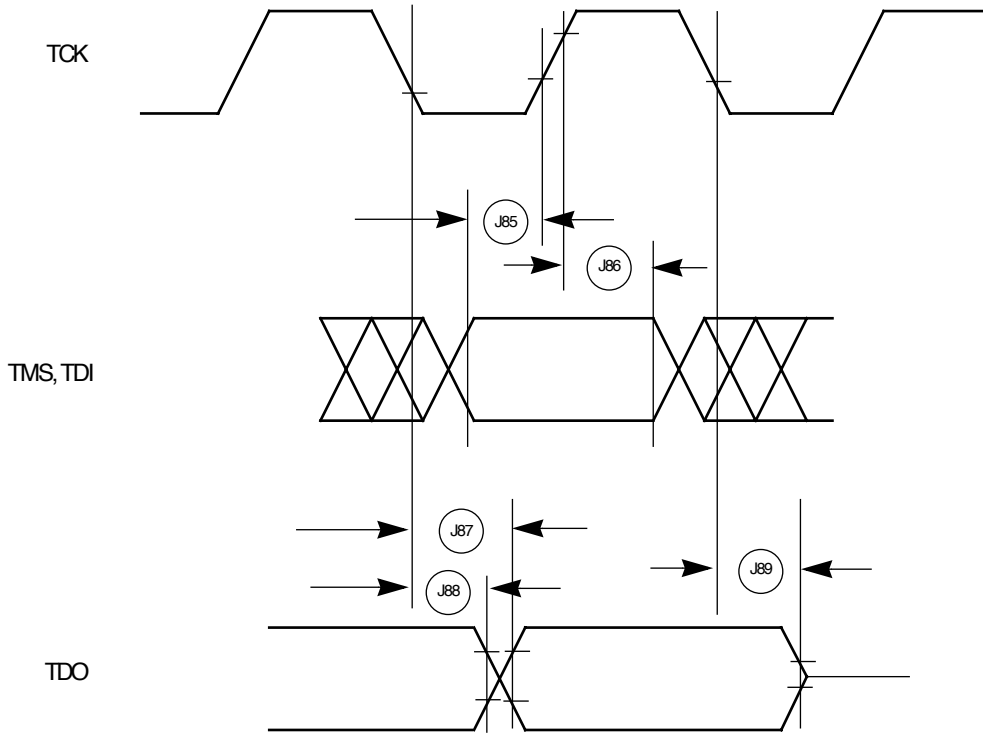
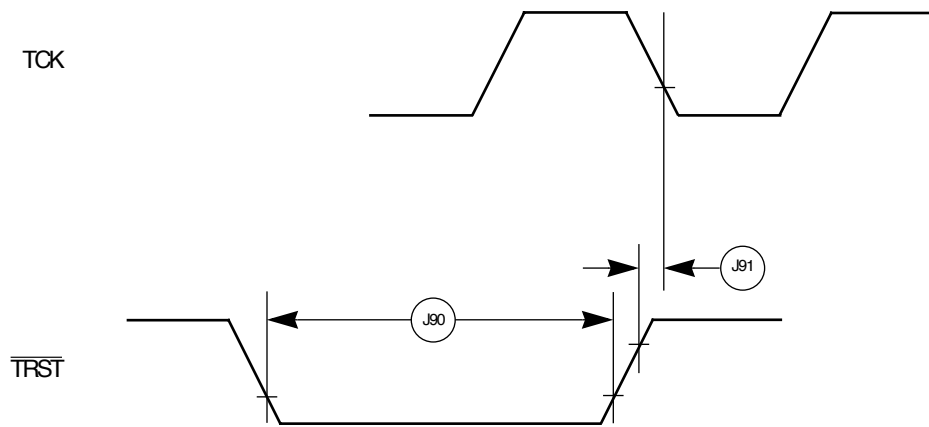


Figure 33. JTAG Test Clock Input Timing Diagram



**Figure 34. JTAG-Test Access Port Timing Diagram**



**Figure 35. JTAG-TRST Timing Diagram**

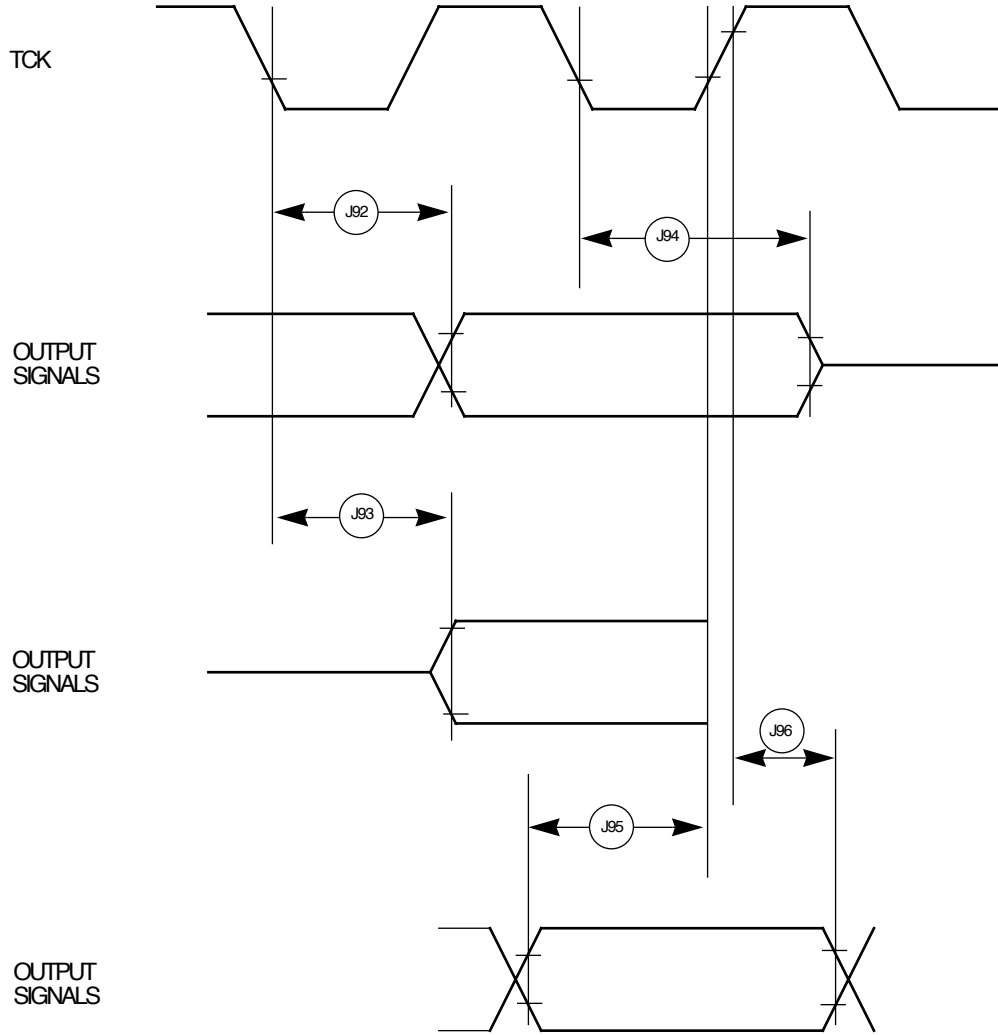
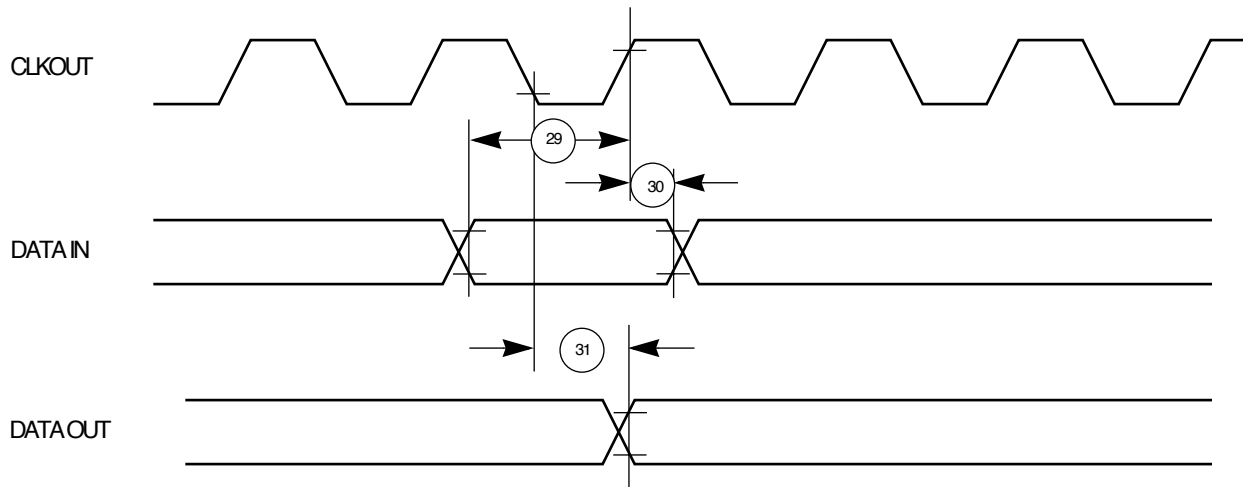


Figure 36. Boundary Scan (JTAG) Timing Diagram

**COMMUNICATION ELECTRICAL CHARACTERISTICS**

**Table 8. Parallel Input/Output Port Timing**

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 29  | Data-in setup time to clock high                                      | 20    | —   | 15    | —   | 15    | —   | ns   |
| 30  | Data-in hold time from clock high                                     | 10    | —   | 7.5   | —   | 7.5   | —   | ns   |
| 31  | Clock high to data-out valid (CPU writes data, control, or direction) | —     | 25  | —     | 25  | —     | 25  | ns   |



**Figure 37. Parallel Input/Output Data-In/Data-Out Timing Diagram**



Table 9. IDMA Timing

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 40  | $\overline{DREQ}$ setup time to clock high                        | 12    | —   | 7     | —   | 7     | —   | nsec |
| 41  | $\overline{DREQ}$ hold time from clock high                       | 5     | —   | 3     | —   | 3     | —   | nsec |
| 42  | $\overline{SDACK}$ assertion delay from clock high                | —     | 20  | —     | 12  | —     | 12  | nsec |
| 43  | $\overline{SDACK}$ negation delay from clock low                  | —     | 20  | —     | 12  | —     | 12  | nsec |
| 44  | $\overline{SDACK}$ negation delay from $\overline{TA}$ low        | —     | 25  | —     | 20  | —     | 20  | nsec |
| 45  | $\overline{SDACK}$ negation delay from clock high                 | —     | 20  | —     | 15  | —     | 15  | nsec |
| 46  | $\overline{TA}$ assertion to falling edge of the clock setup time | 12    | —   | 7     | —   | 7     | —   | nsec |

NOTE: Applies to external  $\overline{TA}$ .

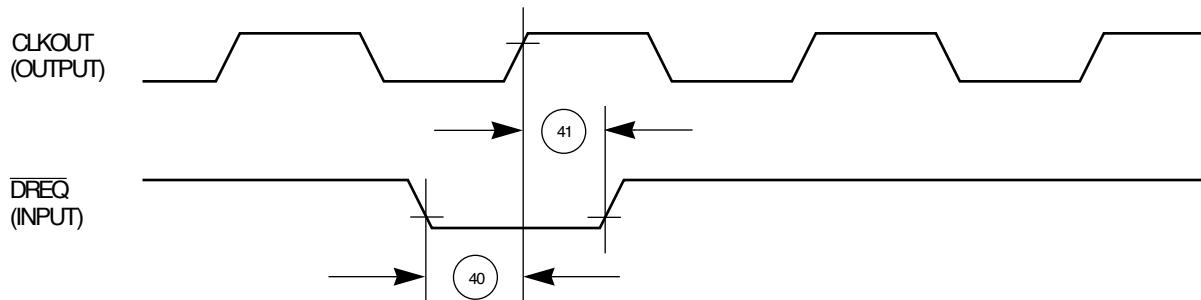


Figure 38. IDMA External Requests Timing Diagram

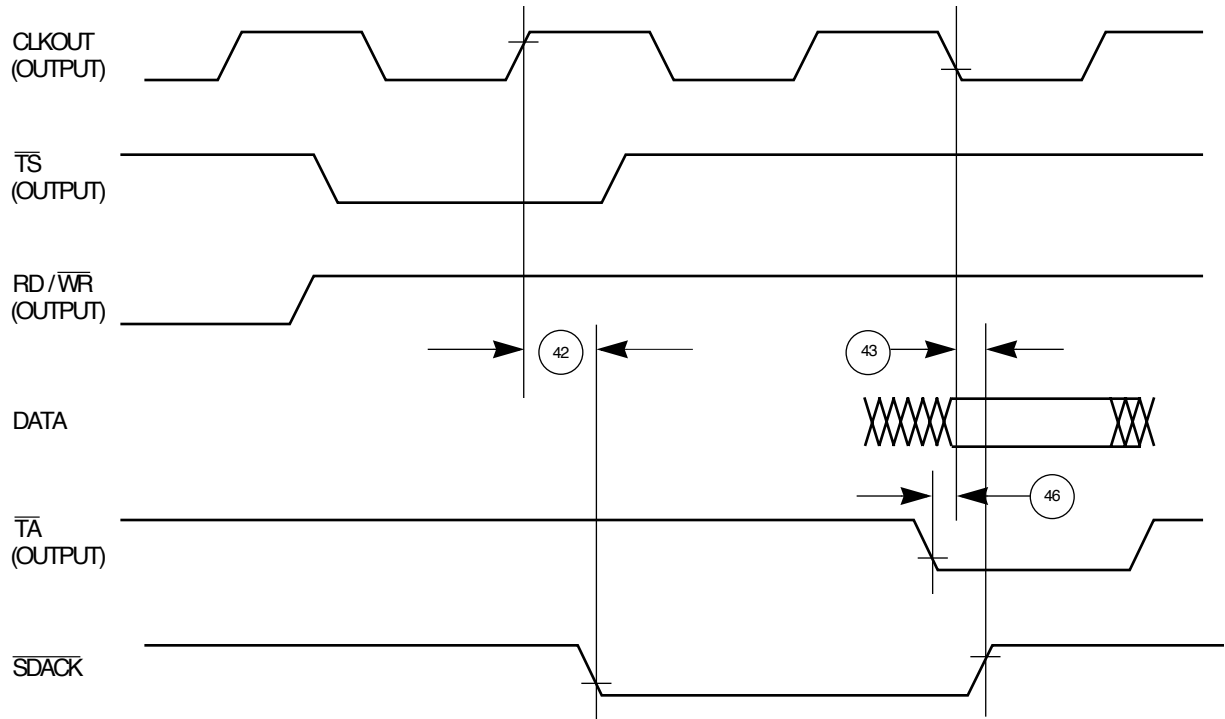


Figure 39.  $\overline{SDACK}$  Timing Diagram—Peripheral Write,  $\overline{TA}$  Sampled Low at the Falling Edge of the Clock

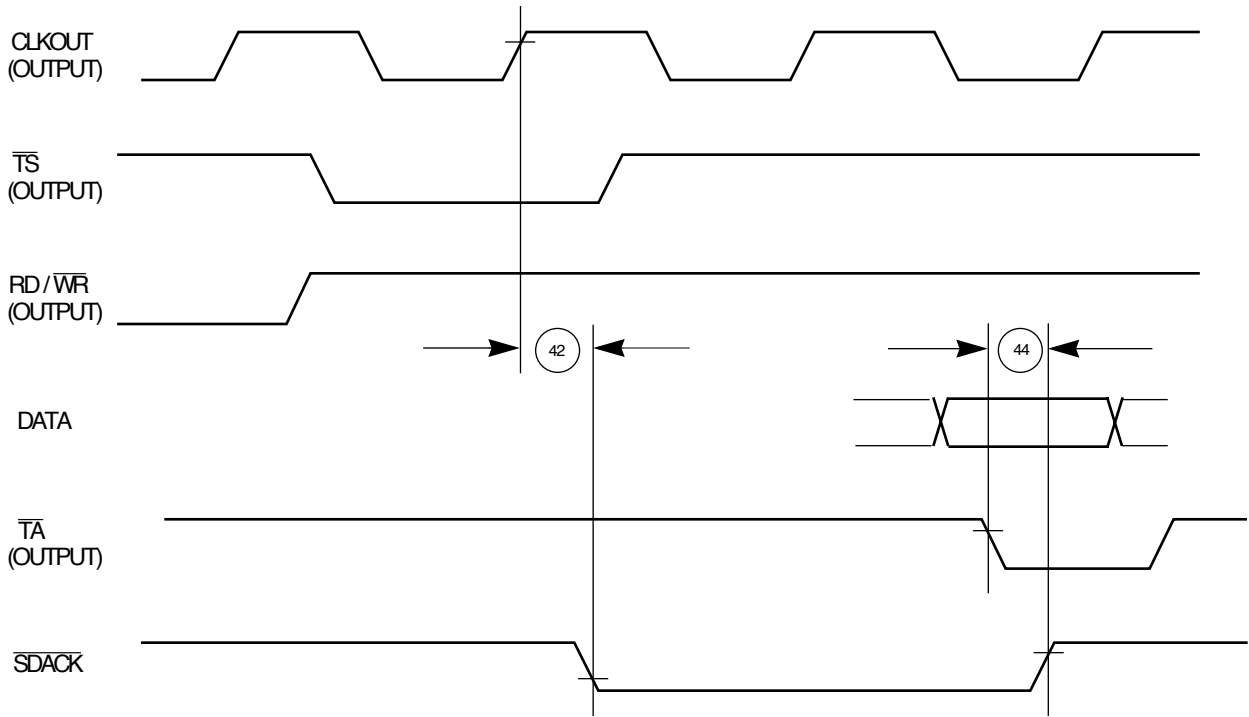


Figure 40.  $\overline{SDACK}$  Timing Diagram—Peripheral Write,  $\overline{TA}$  Sampled High at the Falling Edge of the Clock

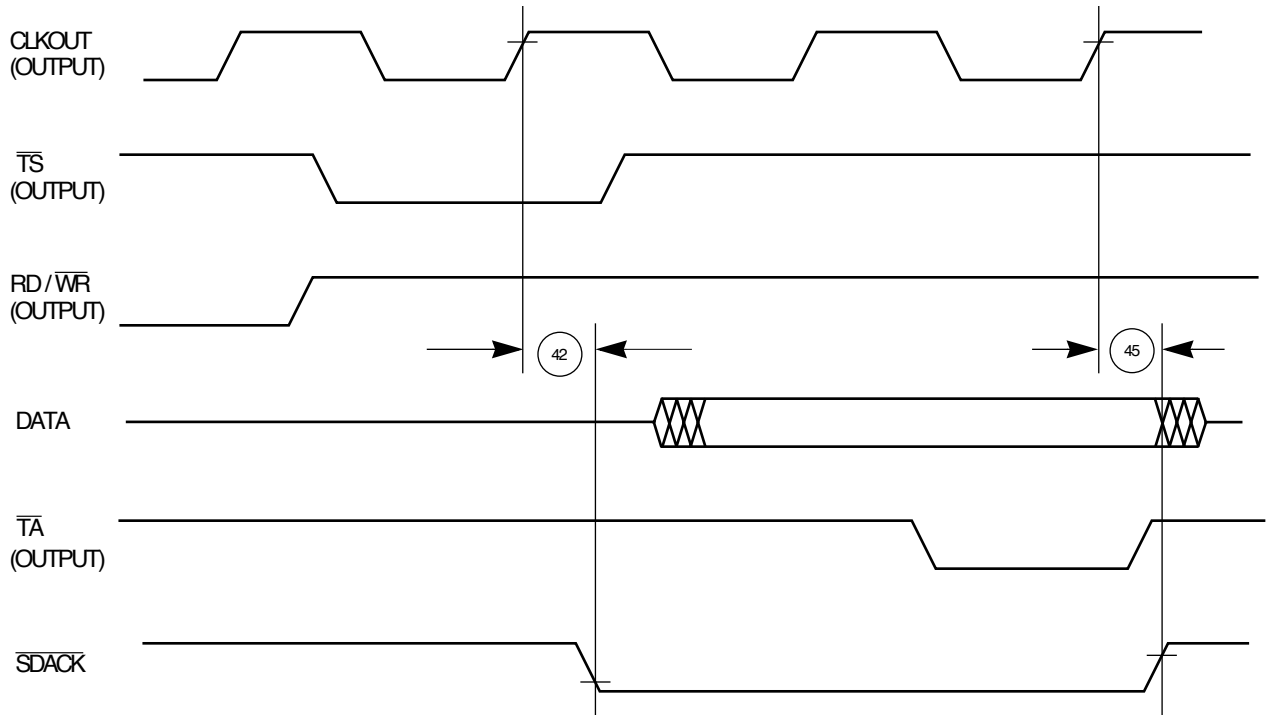
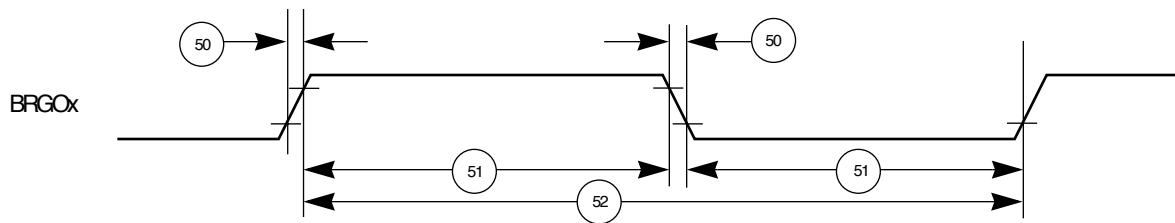


Figure 41.  $\overline{SDACK}$  Timing Diagram—Peripheral Read

**Table 10. Baud Rate Generator Timing**

| NUM | CHARACTERISTIC           | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|--------------------------|-------|-----|-------|-----|-------|-----|------|
|     |                          | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 50  | BRGO rise and fall times | —     | 10  | —     | 10  | —     | 10  | ns   |
| 51  | BRGO duty cycle          | 40    | 60  | 40    | 60  | 40    | 60  | %    |
| 52  | BRGO cycle               | 40    | —   | 40    | —   | 40    | —   | ns   |



**Figure 42. Baud Rate Generator Timing Diagram**

Table 11. General-Purpose Timers Timing

| NUM | CHARACTERISTIC                                     | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|--|-------|-----|-------|-----|-------|-----|------|
|     |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 61  | TIN/ $\overline{\text{TGATE}}$ rise and fall times | 12    | 10  | 7     | 10  | 7     | 10  | ns   |
| 62  | TIN/ $\overline{\text{TGATE}}$ low time            | 5     | 1   | 3     | 1   | 3     | 1   | clk  |
| 63  | TIN/ $\overline{\text{TGATE}}$ high time           | —     | 20  | —     | 12  | —     | 12  | clk  |
| 64  | TIN/ $\overline{\text{TGATE}}$ cycle time          | —     | 20  | —     | 12  | —     | 12  | clk  |
| 65  | CLKO low to $\overline{\text{TOU}}$ valid          | —     | 25  | —     | 20  | —     | 20  | ns   |

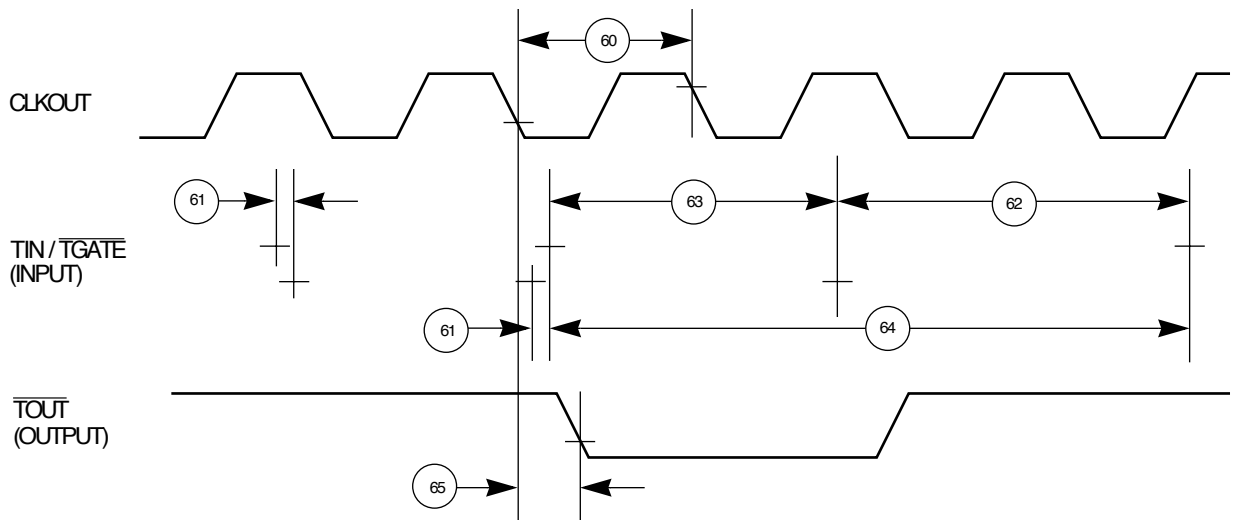


Figure 43. General-Purpose Timers Timing Diagram

**Table 12. Serial Interface Timing**

| NUM | CHARACTERISTIC  | 25MHZ |      | 40MHZ |     | 50MHZ |     | UNIT   |
|-----|---|-------|------|-------|-----|-------|-----|--------|
|     |   | MIN   | MAX  | MIN   | MAX | MIN   | MAX |        |
| 70  | L1RCLK and L1TCLK frequency (DSC=0) <sup>1,3</sup>                | —     | 10   | —     | 10  | —     | 10  | MHz    |
| 71  | L1RCLK and L1TCLK width low (DSC=0) <sup>3</sup>                  | P+10  | —    | P+10  | —   | P+10  | —   | ns     |
| 71a | L1RCLK and L1TCLK width high (DSC=0) <sup>2</sup>                 | P+10  | —    | P+10  | —   | P+10  | —   | ns     |
| 72  | L1TXD, L1ST(1–8), L1RQ, L1CLKO rise and fall times                | —     | 15   | —     | 15  | —     | 15  | ns     |
| 73  | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)            | 20    | —    | 20    | —   | 20    | —   | ns     |
| 74  | L1CLK edge to L1RSYNC and L1TSYNC invalid (SYNC hold time)        | 35    | —    | 35    | —   | 35    | —   | ns     |
| 75  | L1RSYNC and L1TSYNC rise and fall times                           | —     | 15   | —     | 15  | —     | 15  | ns     |
| 76  | L1RXD valid to L1CLK edge (L1RXD setup time)                      | 42    | —    | 42    | —   | 42    | —   | ns     |
| 77  | L1CLK edge to L1RXD invalid (L1RXD hold time)                     | 35    | —    | 35    | —   | 35    | —   | ns     |
| 78  | L1CLK edge to L1ST(1–8) valid                                     | 10    | 45   | 10    | 45  | 10    | 45  | ns     |
| 78a | L1SYNC valid to L1ST(1–8) valid <sup>4</sup>                      | 10    | 45   | 10    | 45  | 10    | 45  | ns     |
| 79  | L1CLK edge to L1ST(1–8) invalid                                   | 10    | 45   | 10    | 45  | 10    | 45  | ns     |
| 80  | L1CLK edge to L1TXD valid   | 10    | 65   | 10    | 65  | 10    | 65  | ns     |
| 80a | L1TSYNC valid to L1TXD valid <sup>4</sup>                         | 10    | 65   | 10    | 65  | 10    | 65  | ns     |
| 81  | L1CLK edge to L1TXD high impedance                                | 0     | 42   | 0     | 42  | 0     | 42  | ns     |
| 82  | L1RCLK and L1TCLK frequency (DSC=1)                               | —     | 12.5 | —     | 16  | —     | 16  | MHz    |
| 83  | L1RCLK and L1TCLK width low (DSC=1)                               | P+10  | —    | P+10  | —   | P+10  | —   | ns     |
| 83a | L1RCLK and L1TCLK width high (DSC=1) <sup>2</sup>                 | P+10  | —    | P+10  | —   | P+10  | —   | ns     |
| 84  | L1CLK edge to L1CLKO valid (DSC=1)                                | —     | 30   | —     | 30  | —     | 30  | ns     |
| 85  | L1RQ valid before falling edge of L1TSYNC <sup>3</sup>            | 1     | —    | 1     | —   | 1     | —   | L1TCLK |
| 86  | L1GR setup time <sup>3</sup>                                      | 42    | —    | 42    | —   | 42    | —   | ns     |
| 87  | L1GR hold time <sup>3</sup>                                       | 42    | —    | 42    | —   | 42    | —   | ns     |
| 88  | L1CLK edge to L1SYNC valid (FSD = 00, CNT = 0000, BYT = 0, DSC=0) | —     | 0    | —     | 0   | —     | 0   | ns     |

NOTES:

1. The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2. Where P=1/CLKO1. For a 25MHz CLKO1 rate, P=40ns.
3. These electrical specifications are only valid for IDL mode.
4. The strobes and TXD2 on the first bit of the frame becomes valid after L1CLK edge or L1SYNC, whichever is later.

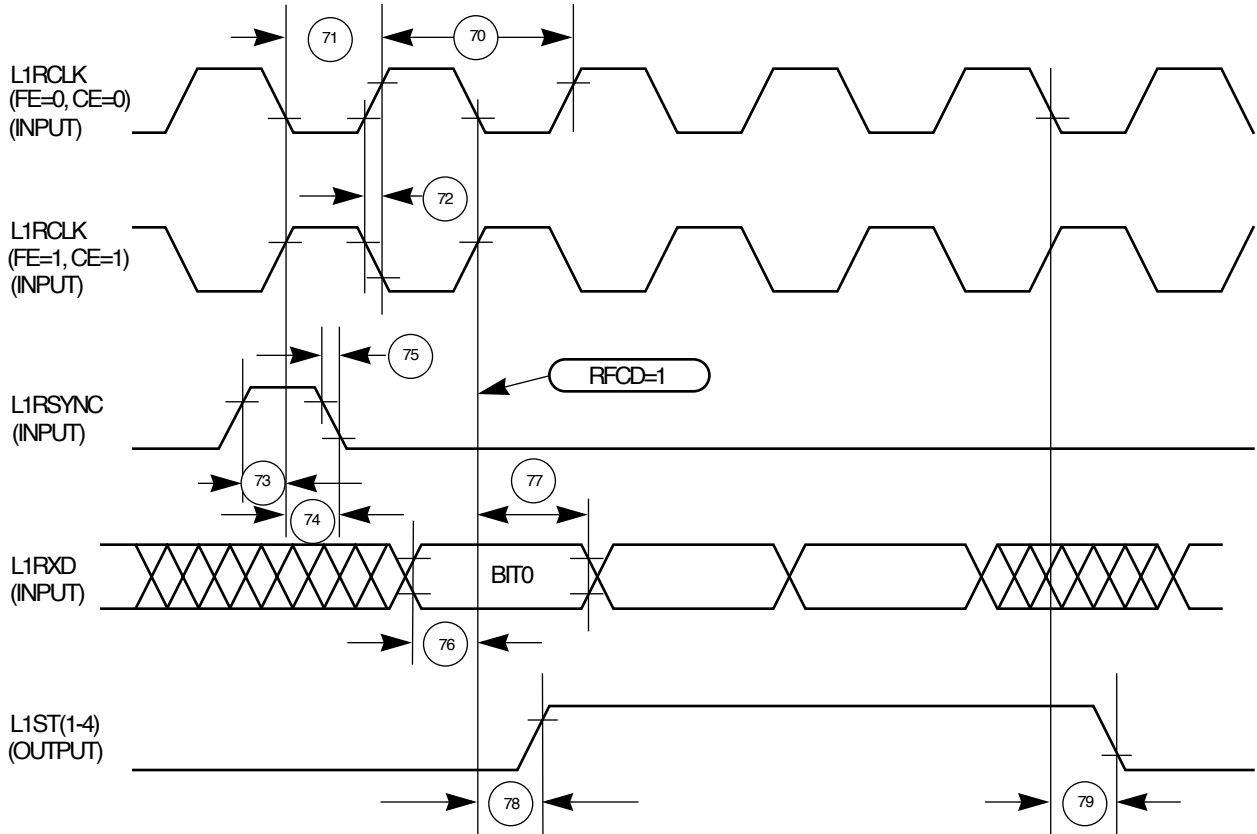


Figure 44. Serial Interface Receive Timing Diagram With Normal Clocking (DSC = 0)



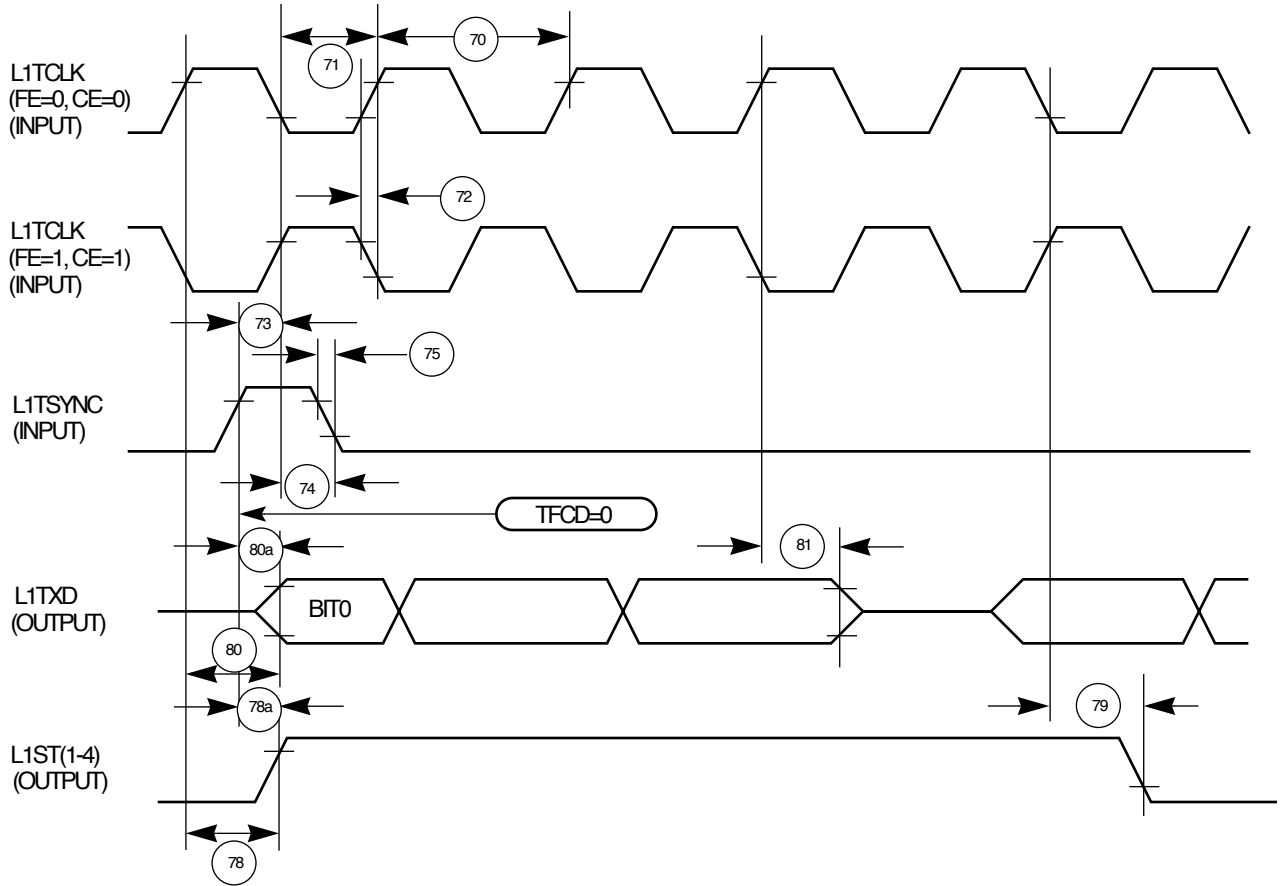


Figure 45. Serial Interface Transmit Timing Diagram

**Table 13. Serial Communication Controller in NMSI External Timing**

| NUM | CHARACTERISTIC  | 25MHZ                  |     | 40MHZ                  |     | 50MHZ                  |     | UNIT |
|-----|---|------------------------|-----|------------------------|-----|------------------------|-----|------|
|     |   | MIN                    | MAX | MIN                    | MAX | MIN                    | MAX |      |
| 100 | RCLK1 and TCLK1 width high <sup>1</sup>                           | CLKOUT <sub>F</sub>    | —   | CLKOUT <sub>F</sub>    | —   | CLKOUT <sub>F</sub>    | —   | MHz  |
| 101 | RCLK1 and TCLK1 width low   | CLKOUT <sub>+5ns</sub> | —   | CLKOUT <sub>+5ns</sub> | —   | CLKOUT <sub>+5ns</sub> | —   | ns   |
| 102 | RCLK1 and TCLK1 rise and fall times                               | —                      | 15  | —                      | 15  | —                      | 15  | ns   |
| 103 | TXD2 active delay (from TCLK1 falling edge)                       | 0                      | 50  | 0                      | 50  | 0                      | 50  | ns   |
| 104 | $\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge) | 0                      | 50  | 0                      | 50  | 0                      | 50  | ns   |
| 105 | $\overline{CTS1}$ setup time to TCLK1 rising edge                 | 5                      | —   | 5                      | —   | 5                      | —   | ns   |
| 106 | RXD2 setup time to RCLK1 rising edge                              | 5                      | —   | 5                      | —   | 5                      | —   | ns   |
| 107 | RXD2 hold time from RCLK1 rising edge <sup>2</sup>                | 5                      | —   | 5                      | —   | 5                      | —   | ns   |
| 108 | $\overline{CD1}$ setup time to RCLK1 rising edge                  | 5                      | —   | 5                      | —   | 5                      | —   | ns   |

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2. Applies to  $\overline{CD}$  and  $\overline{CTS}$  hold time when they are used as external sync signals.

Table 14. Serial Communication Controller in NMSI Internal Timing

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 100 | RCLK1 and TCLK1 frequency <sup>1</sup>                            | 0     | 8.3 | 0     | 13  | 0     | 16  | MHz  |
| 102 | RCLK1 and TCLK1 rise and all times                                | —     | —   | —     | —   | —     | —   | ns   |
| 103 | TXD2 active delay (from TCLK1 falling edge)                       | 0     | 30  | 0     | 30  | 0     | 30  | ns   |
| 104 | $\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge) | 0     | 30  | 0     | 30  | 0     | 30  | ns   |
| 105 | $\overline{CTS1}$ setup time to TCLK1 rising edge                 | 40    | —   | 40    | —   | 40    | —   | ns   |
| 106 | RXD2 setup time to RCLK1 rising edge                              | 40    | —   | 40    | —   | 40    | —   | ns   |
| 107 | RXD2 hold time from RCLK1 rising edge <sup>2</sup>                | 0     | —   | 0     | —   | 0     | —   | ns   |
| 108 | $\overline{CD1}$ setup time to RCLK1 rising edge                  | 40    | —   | 40    | —   | 40    | —   | ns   |

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2. Applies to  $\overline{CD}$  and  $\overline{CTS}$  hold time when they are used as external sync signals.

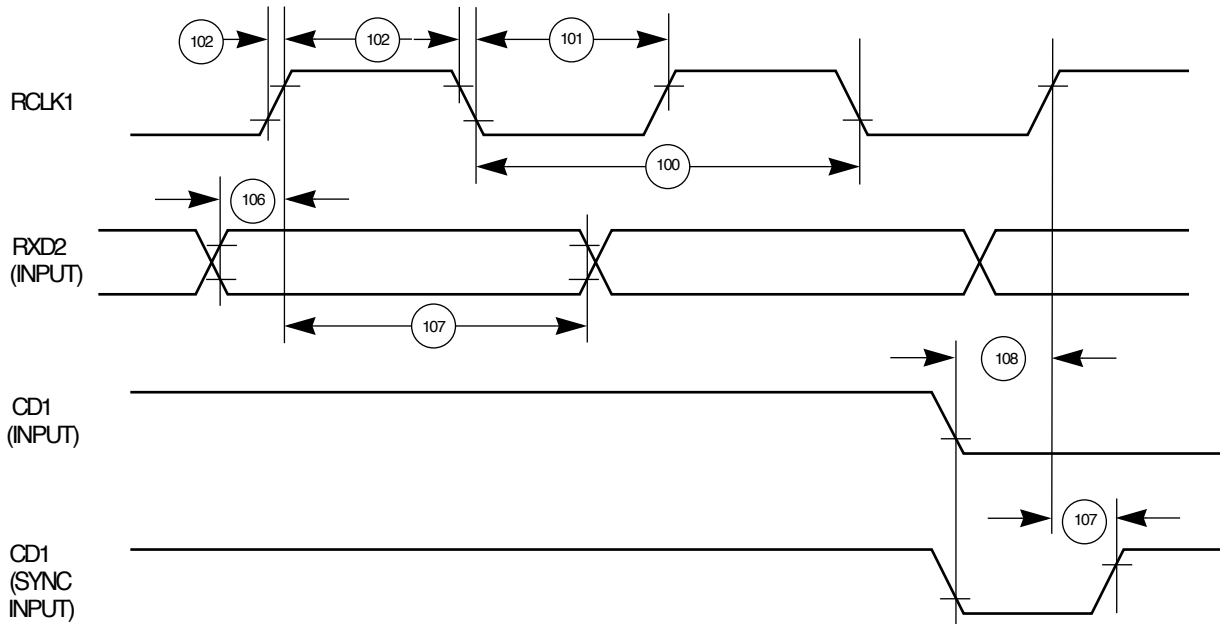


Figure 46. SCC NMSI Receive Timing Diagram

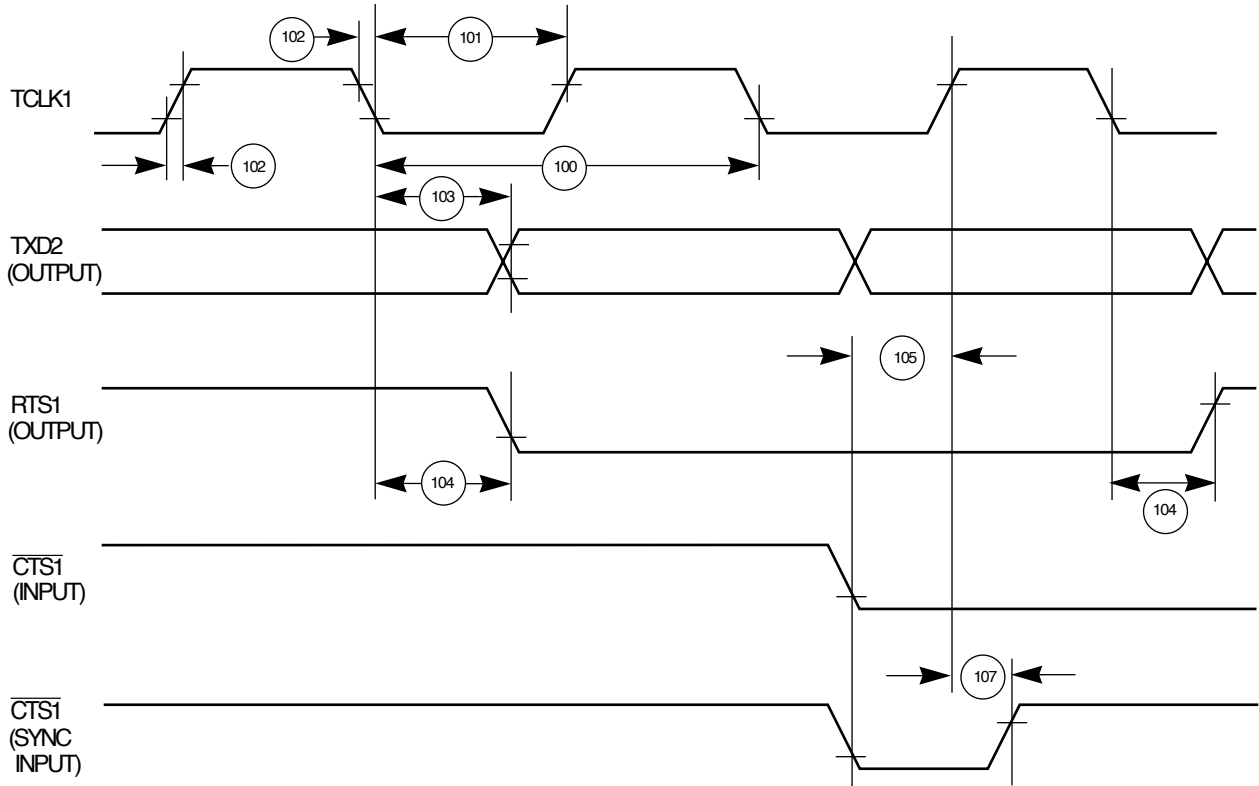


Figure 47. SCC NMSI Transmit Timing Diagram

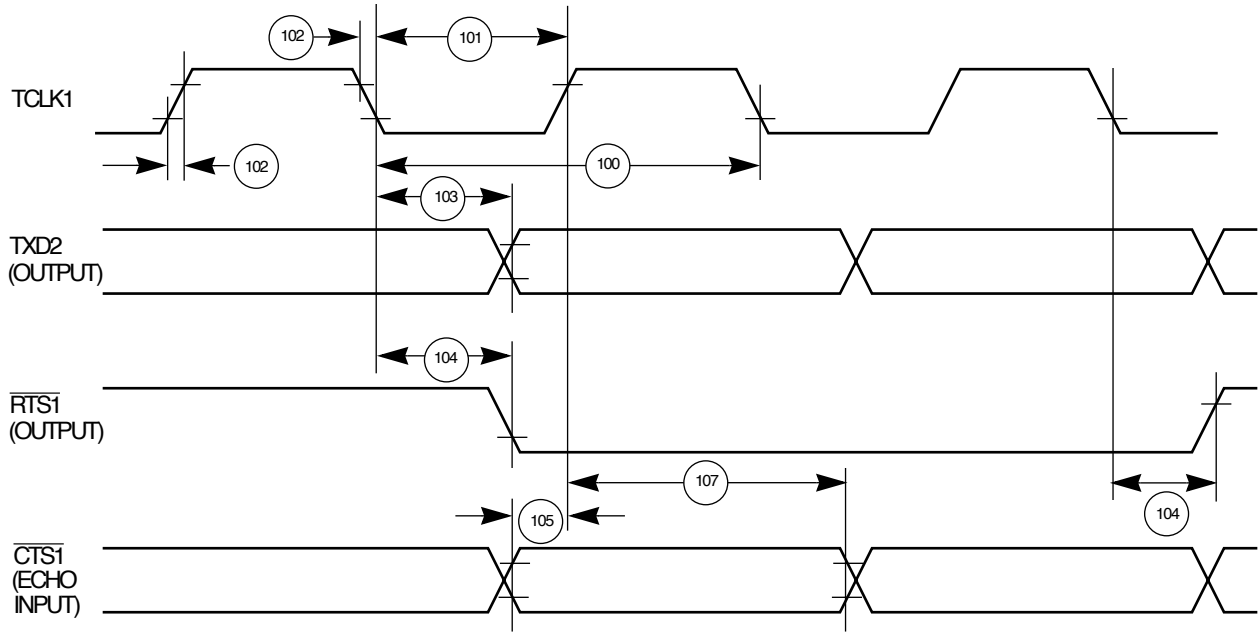


Figure 48. HDLC Bus Timing Diagram

**Table 15. Ethernet Timing**

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 120 | CLSN (CTS2) width high  | 40    | —   | 40    | —   | 40    | —   | ns   |
| 121 | RCLK1 rise and fall times   | —     | 15  | —     | 15  | —     | 15  | ns   |
| 122 | RCLK1 width low   | 40    | —   | 40    | —   | 40    | —   | ns   |
| 123 | RCLK1 clock period <sup>1</sup>                                       | 80    | 120 | 80    | 120 | 80    | 120 | ns   |
| 124 | RXD2 setup time   | 20    | —   | 20    | —   | 20    | —   | ns   |
| 125 | RXD2 hold time  | 5     | —   | 5     | —   | 5     | —   | ns   |
| 126 | RENA (CD2) active delay (from RCLK1 rising edge of the last data bit) | 10    | —   | 10    | —   | 10    | —   | ns   |
| 127 | RENA (CD2) width low  | 100   | —   | 100   | —   | 100   | —   | ns   |
| 128 | TCLK1 rise and fall times   | —     | 15  | —     | 15  | —     | 15  | ns   |
| 129 | TCLK1 width low   | 40    | —   | 40    | —   | 40    | —   | ns   |
| 130 | TCLK1 clock period <sup>1</sup>                                       | 99    | 101 | 99    | 101 | 99    | 101 | ns   |
| 131 | TXD2 active delay (from TCLK1 rising edge)                            | 10    | 50  | 10    | 50  | 10    | 50  | ns   |
| 132 | TXD2 inactive delay (from TCLK1 rising edge)                          | 10    | 50  | 10    | 50  | 10    | 50  | ns   |
| 133 | TENA (RTS2) active delay (from TCLK1 rising edge)                     | 10    | 50  | 10    | 50  | 10    | 50  | ns   |
| 134 | TENA (RTS2) inactive delay (from TCLK1 rising edge)                   | 10    | 50  | 10    | 50  | 10    | 50  | ns   |
| 135 | N/A   |       |     |       |     |       |     |      |
| 136 | N/A   |       |     |       |     |       |     |      |
| 137 | N/A   |       |     |       |     |       |     |      |
| 138 | CLKx low to $\overline{SDACK}$ asserted <sup>2</sup>                  | —     | 20  | —     | 20  | —     | 20  | ns   |
| 139 | CLKx low to $\overline{SDACK}$ negated <sup>3</sup>                   | —     | 20  | —     | 20  | —     | 20  | ns   |

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.
2.  $\overline{SDACK}$  is asserted when the SDMA writes the incoming frame DA into memory.

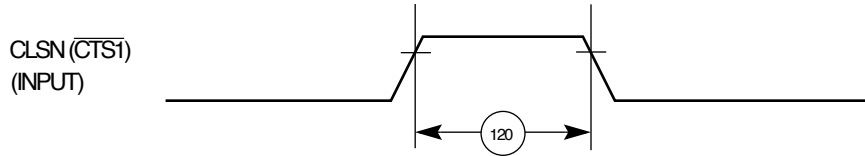


Figure 49. Ethernet Collision Timing Diagram

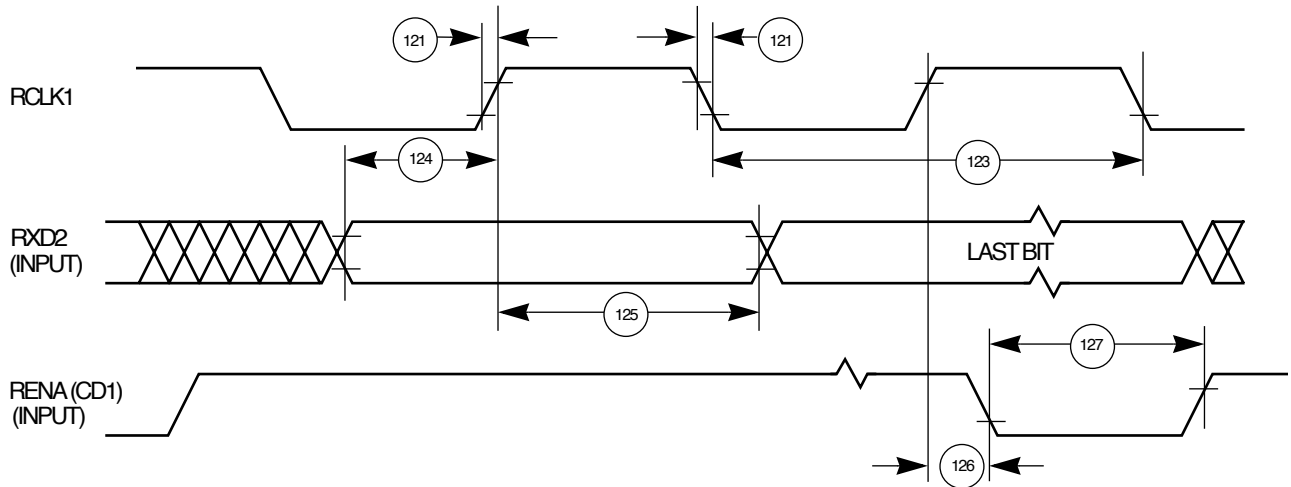
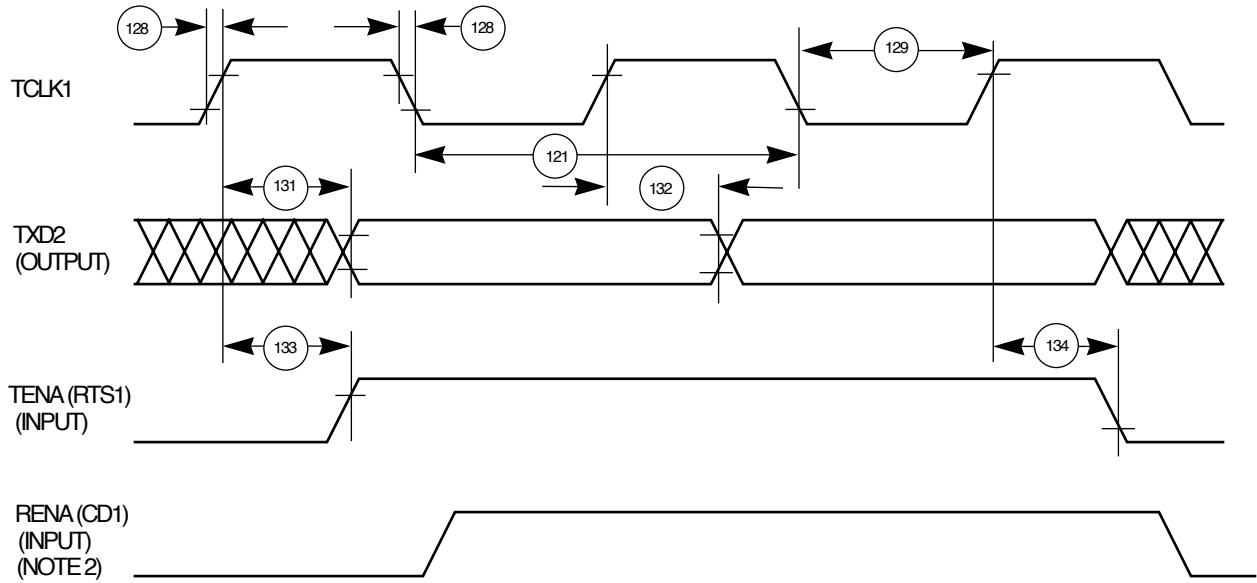


Figure 50. Ethernet Receive Timing Diagram



- NOTES: 1. TRANSMIT CLOCK INVERT (TCI) BIT IN THE GSMR IS SET.  
 2. IF RENA IS DEASSERTED BEFORE TENA, OR RENA IS NOT ASSERTED AT ALL DURING TRANSMIT, THEN THE CSL BIT IS SET IN THE BUFFER DESCRIPTOR AT THE END OF FRAME TRANSMISSION.

**Figure 51. Ethernet Transmit Timing Diagram**



Table 16. Serial Peripheral Interface Master Timing

| NUM | CHARACTERISTIC                      | 25MHZ |       | 40MHZ |       | 50MHZ |       | UNIT |
|-----|-------------------------------------|-------|-------|-------|-------|-------|-------|------|
|     |                                     | MIN   | MAX   | MIN   | MAX   | MIN   | MAX   |      |
| 160 | Master cycle time                   | 4     | 1,024 | 4     | 1,024 | 4     | 1,024 | tcyc |
| 161 | Master clock (SCK) high or low time | 2     | 512   | 2     | 512   | 2     | 512   | tcyc |
| 162 | Master data setup time (inputs)     | 50    | —     | 50    | —     | 50    | —     | ns   |
| 163 | Master data hold time (inputs)      | 0     | —     | 0     | —     | 0     | —     | ns   |
| 164 | Master data valid (after SCK edge)  | —     | 20    | —     | 20    | —     | 20    | ns   |
| 165 | Master data hold time (outputs)     | 0     | —     | 0     | —     | 0     | —     | ns   |
| 166 | Rise time output                    | —     | 15    | —     | 15    | —     | 15    | ns   |
| 167 | Fall time output                    | —     | 15    | —     | 15    | —     | 15    | ns   |

NOTE: The ratio SyncCLK/SMCLK must be greater than or equal to 2/1.

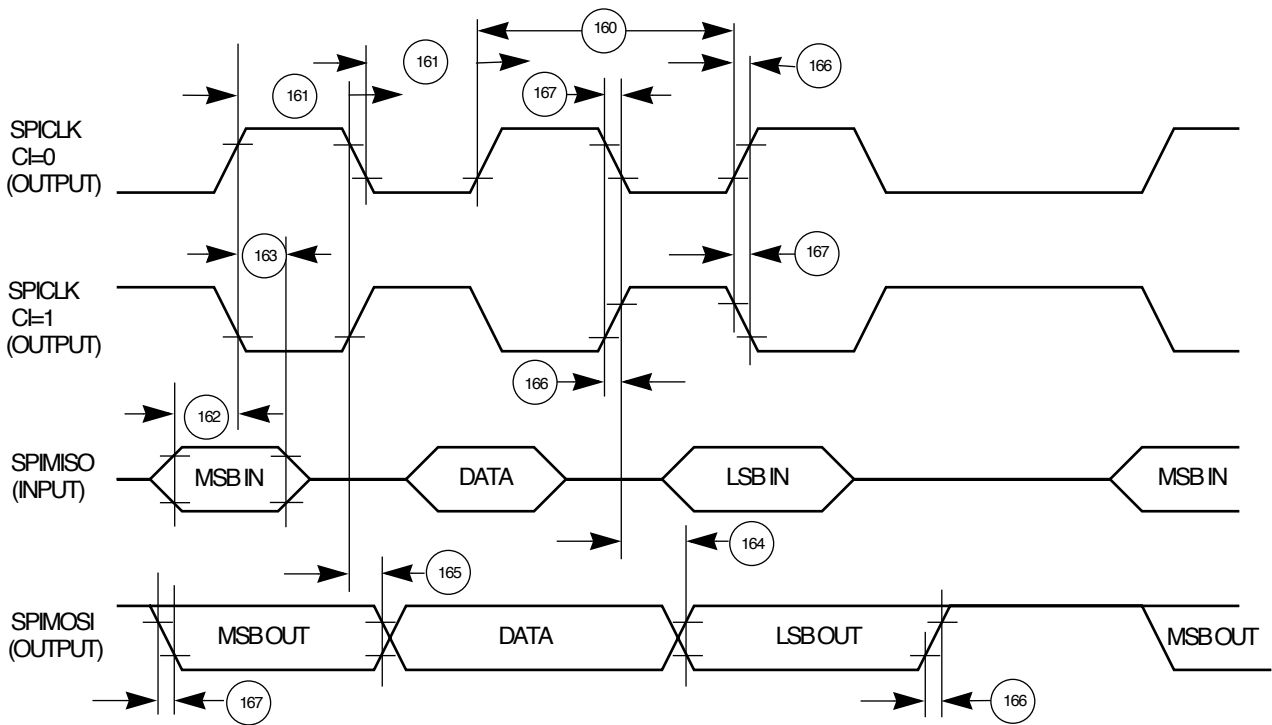


Figure 52. SPI Master (CP=0) Timing Diagram

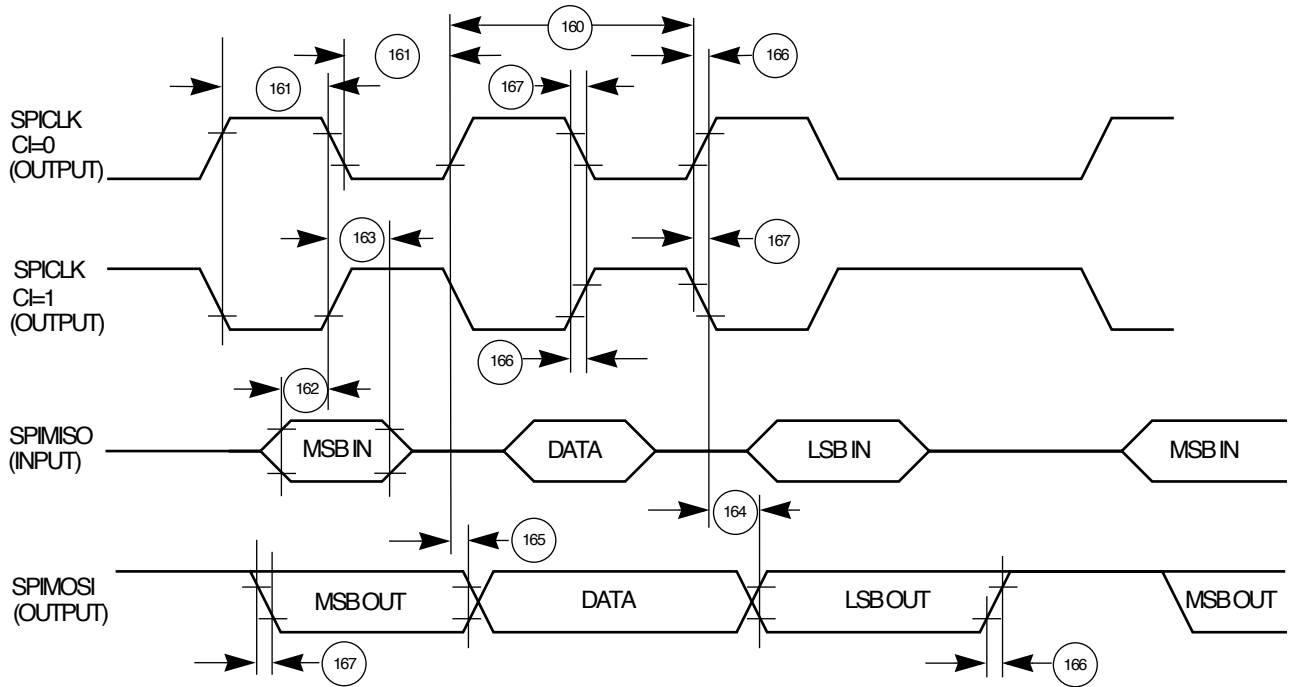


Figure 53. SPI Master (CP=1) Timing Diagram

**Table 17. Serial Peripheral Interface Slave Timing**

| NUM | CHARACTERISTIC  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 170 | Slave cycle time  | 2     | —   | 2     | —   | 2     | —   | tcyc |
| 171 | Slave enable lead time                                      | 15    | —   | 15    | —   | 15    | —   | ns   |
| 172 | Slave enable lag time                                       | 15    | —   | 15    | —   | 15    | —   | ns   |
| 173 | Slave clock (SPICLK) high or low time                       | 1     | —   | 1     | —   | 1     | —   | tcyc |
| 174 | Slave sequential transfer delay (does not require deselect) | 1     | —   | 1     | —   | 1     | —   | tcyc |
| 175 | Slave data setup time (inputs)                              | 20    | —   | 20    | —   | 20    | —   | ns   |
| 176 | Slave data hold time (inputs)                               | 20    | —   | 20    | —   | 20    | —   | ns   |
| 177 | Slave access time   | —     | 50  | —     | 50  | —     | 50  | ns   |
| 178 | Slave SPI MISO disable time                                 | —     | 50  | —     | 50  | —     | 50  | ns   |
| 179 | Slave data valid (after SPICLK edge)                        | —     | 50  | —     | 50  | —     | 50  | ns   |
| 180 | Slave data hold time (outputs)                              | 0     | —   | 0     | —   | 0     | —   | ns   |
| 181 | Rise time (input)   | —     | 15  | —     | 15  | —     | 15  | ns   |
| 182 | Fall time (input)   | —     | 15  | —     | 15  | —     | 15  | ns   |

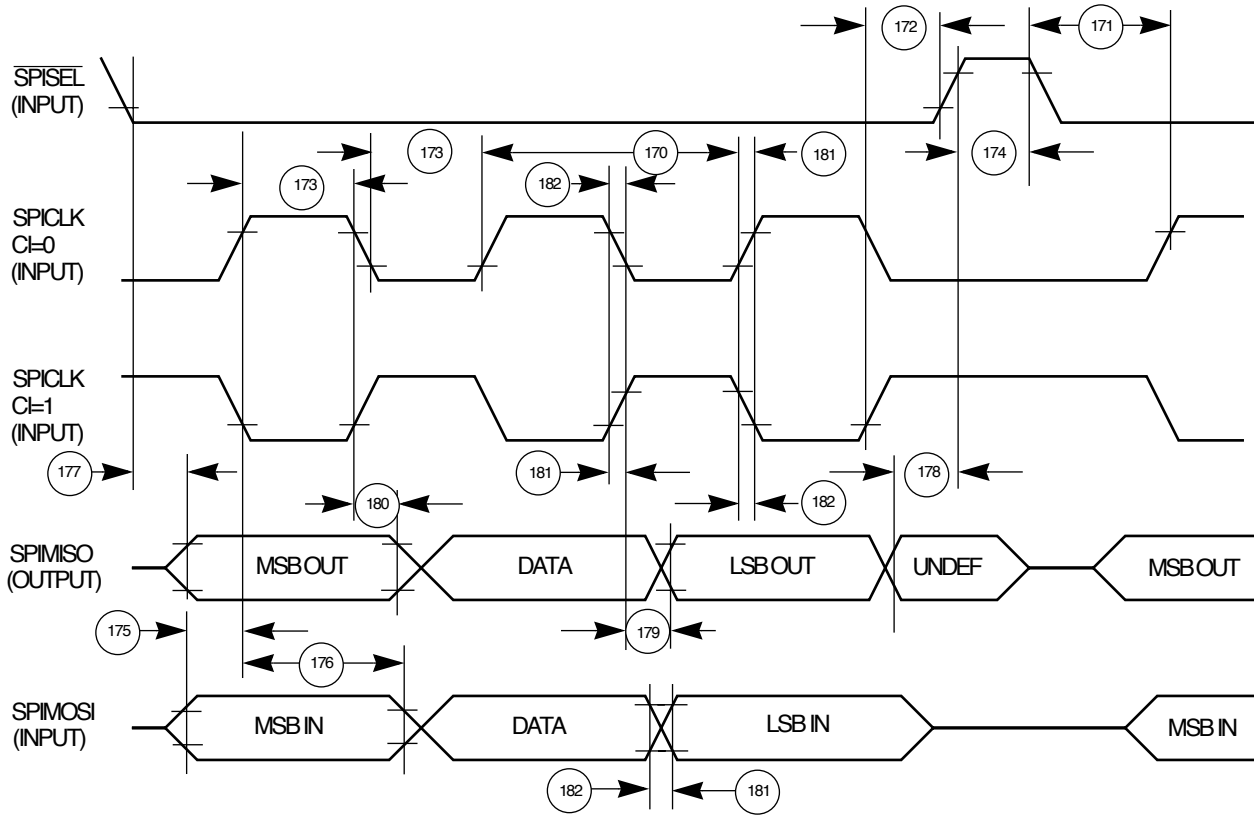


Figure 54. SPI Slave (CP=0) Timing Diagram

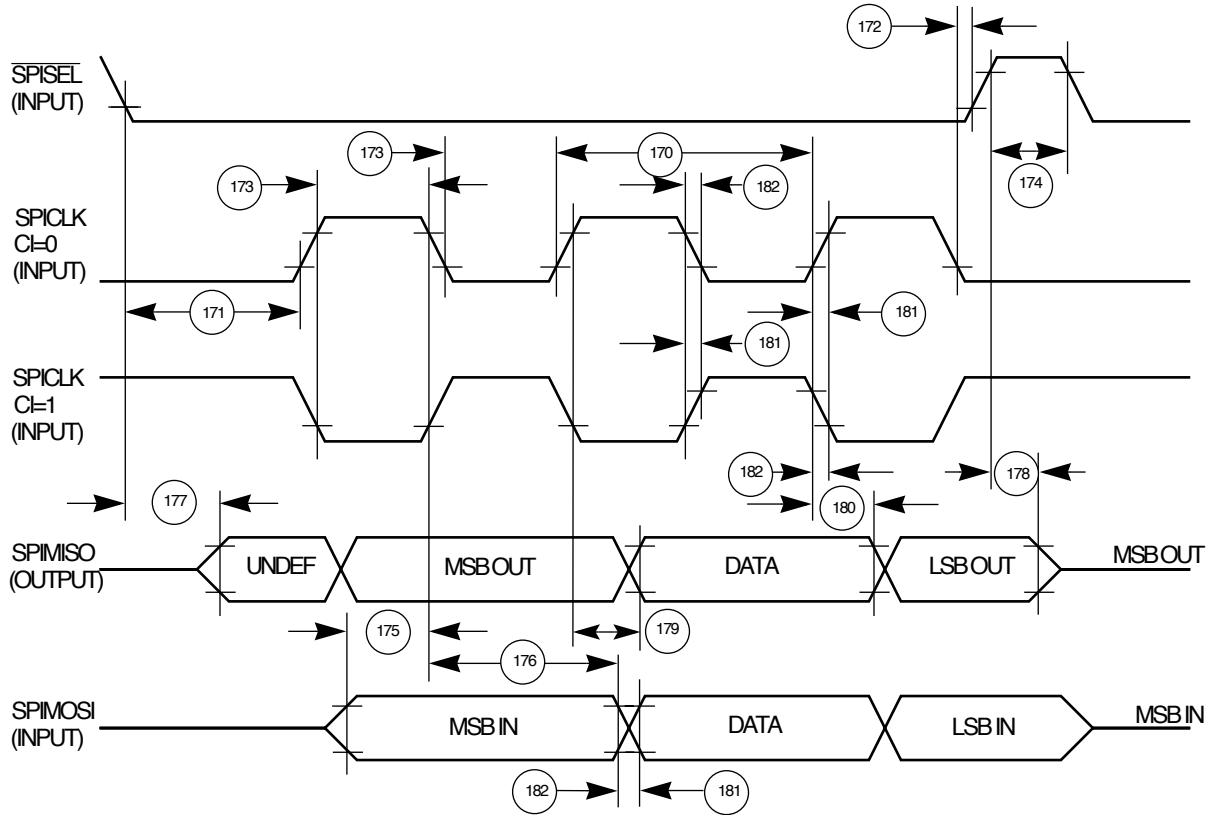


Figure 55. SPI Slave (CP=1) Timing Diagram

**Table 18. I<sup>2</sup>C Timing—SCL < 100 kHz**

| NUM | CHARACTERISTIC                      | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|-------------------------------------|-------|-----|-------|-----|-------|-----|------|
|     |                                     | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 200 | SCL clock frequency (slave)         | 0     | 100 | 0     | 100 | 0     | 100 | kHz  |
| 200 | SCL clock frequency (master)        | 1.5   | 100 | 1.5   | 100 | 1.5   | 100 | kHz  |
| 202 | Bus free time between transmissions | 4.7   | —   | 4.7   | —   | 4.7   | —   | μs   |
| 203 | Low period of SCL                   | 4.7   | —   | 4.7   | —   | 4.7   | —   | μs   |
| 204 | High period of SCL                  | 4.0   | —   | 4.0   | —   | 4.0   | —   | μs   |
| 205 | Start condition setup time          | 4.7   | —   | 4.7   | —   | 4.7   | —   | μs   |
| 206 | Start condition hold time           | 4.0   | —   | 4.0   | —   | 4.0   | —   | μs   |
| 207 | Data hold time                      | 0     | —   | 0     | —   | 0     | —   | μs   |
| 208 | Data setup time                     | 250   | —   | 250   | —   | 250   | —   | ns   |
| 209 | SDL/SCL rise time                   | —     | 1   | —     | 1   | —     | 1   | μs   |
| 210 | SDL/SCL fall time                   | —     | 300 | —     | 300 | —     | 300 | ns   |
| 211 | STOP condition setup time           | 4.7   | —   | 4.7   | —   | 4.7   | —   | μs   |

NOTE: SCL frequency is given by  $SCL = BRGCLK\_frequency / ((BRG\ register + 3) * pre\_scaler * 2)$ .  
The ratio  $SyncClk / (BRGCLK / pre\_scaler)$  must be greater than or equal to 4/1.

**Table 19. I<sup>2</sup>C Timing—SCL > 100 kHz**

| NUM | CHARACTERISTIC                      | MINIMUM        | MAXIMUM       | UNIT |
|-----|-------------------------------------|----------------|---------------|------|
| 200 | SCL clock frequency (slave)         | 0              | BRGCLK/48     | Hz   |
| 200 | SCL clock frequency (master)        | BRGCLK/16512   | BRGCLK/48     | Hz   |
| 202 | Bus free time between transmissions | 1/(2.2 * fSCL) | —             | sec  |
| 203 | Low period of SCL                   | 1/(2.2 * fSCL) | —             | sec  |
| 204 | High period of SCL                  | 1/(2.2 * fSCL) | —             | sec  |
| 205 | Start condition setup time          | 1/(2.2 * fSCL) | —             | sec  |
| 206 | Start condition hold time           | 1/(2.2 * fSCL) | —             | sec  |
| 207 | Data hold time                      | 0              | —             | sec  |
| 208 | Data setup time                     | 1/(40 * fSCL)  | —             | sec  |
| 209 | SDL/SCL rise time                   | —              | 1/(10 * fSCL) | sec  |
| 210 | SDL/SCL fall time                   | —              | 1/(33 * fSCL) | sec  |
| 211 | Stop condition setup time           | 1/(2.2 * fSCL) | —             | sec  |

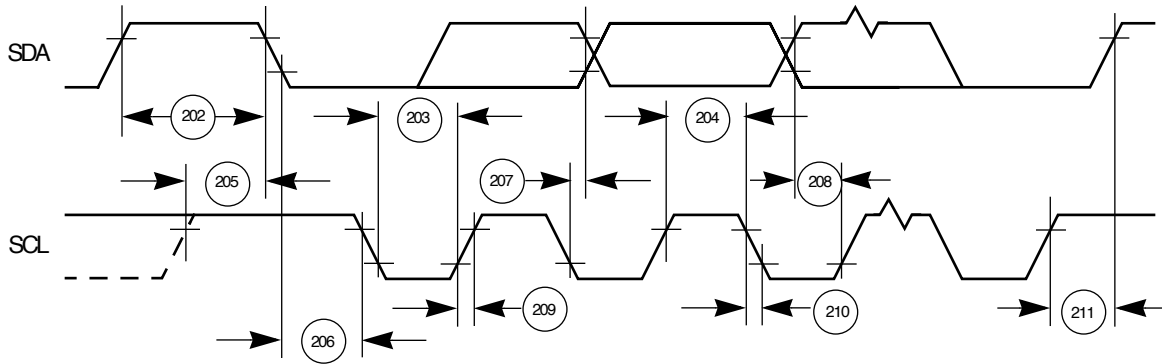
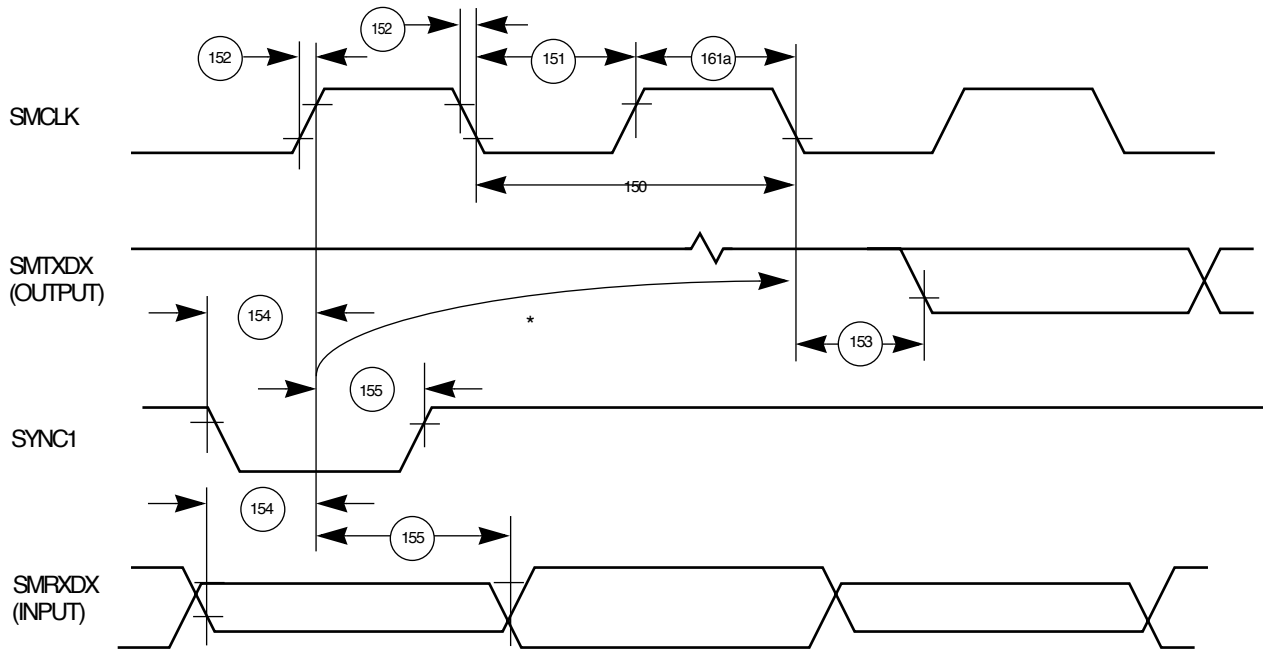


Figure 56. I<sup>2</sup>C Bus Timing Diagram

Table 20. Serial Management Controller Timing

| NUM  | CHARACTERISTIC                               | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|------|--|-------|-----|-------|-----|-------|-----|------|
|      |  | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 150  | CLK1 clock period                            | 100   | —   | 100   | —   | 100   | —   | ns   |
| 151  | CLK1 width low                               | 50    | —   | 50    | —   | 50    | —   | ns   |
| 151A | CLK1 width high                              | 50    | —   | 50    | —   | 50    | —   | ns   |
| 152  | CLK1 rise and fall times                     | —     | 15  | —     | 15  | —     | 15  | ns   |
| 153  | SMTXDx active delay (from CLK1 falling edge) | 10    | 50  | 10    | 50  | 10    | 50  | ns   |
| 154  | SMRXDx/SYNC1 setup time                      | 20    | —   | 20    | —   | 20    | —   | ns   |
| 155  | SMRXDx/SYNC1 hold time                       | 5     | —   | 5     | —   | 5     | —   | ns   |

NOTE: The ratio SyncCLK/SMCLK must be greater than or equal to 2/1.



NOTE: \* THIS DELAY IS EQUAL TO AN INTEGER NUMBER OF "CHARACTER LENGTH" CLOCKS.

Figure 57. SMC Transparent Timing Diagram



**Table 21. LCD Controller Timing**

| NUM | CHARACTERISTIC   | 25MHZ |       | 40MHZ |       | 50MHZ |       | UNIT |
|-----|--|-------|-------|-------|-------|-------|-------|------|
|     |  | MIN   | MAX   | MIN   | MAX   | MIN   | MAX   |      |
| 220 | Shift clock cycle time   | 40    | —     | 40    | —     | 40    | —     | nsec |
| 221 | Shift clock high time  | 20    | —     | 20    | —     | 20    | —     | nsec |
| 223 | CLOCK/HSYNC/VSYNC/ $\overline{OE}$ rise and fall times         | —     | 10    | —     | 10    | —     | 10    | nsec |
| 224 | Data valid delay from shift clock high                         | —     | 15    | —     | 15    | —     | 15    | nsec |
| 225 | VSYNC to HSYNC setup time <sup>1</sup>                         | 5     | —     | 5     | —     | 5     | —     | T    |
| 226 | VSYNC hold time  | 1     | —     | 1     | —     | 1     | —     | T    |
| 227 | HSYNC pulse width  | 4     | —     | 4     | —     | 4     | —     | T    |
| 228 | Time from clock falling edge to HSYNC rising edge              | 4.5   | —     | 4.5   | —     | 4.5   | —     | T    |
| 229 | Time from HSYNC falling edge to clock rising edge <sup>2</sup> | 4     | —     | 4     | —     | 4     | —     | T    |
| 230 | AC active delay  | —     | 25    | —     | 25    | —     | 25    | nsec |
| 231 | VSYNC pulse width (TFT)  | 1     | 16    | 1     | 16    | 1     | 16    | Line |
| 232 | HSYNC to $\overline{OE}$ delay <sup>3</sup>                    | 4     | —     | 4     | —     | 4     | —     | T    |
| 233 | $\overline{OE}$ to HSYNC delay                                 | 4     | —     | 4     | —     | 4     | —     | T    |
| 234 | VSYNC to $\overline{OE}$ delay (TFT)                           | 0     | 1,023 | 0     | 1,023 | 0     | 1,023 | T    |
| 235 | VSYNC/HSYNC/ $\overline{OE}$ active delay (TFT)                | —     | 15    | —     | 15    | —     | 15    | nsec |
| 236 | Wait between frames <sup>4</sup>                               | WBF   | —     | WBF   | —     | WBF   | —     | Line |

NOTES:

1. T = shift clock cycle (220).
2. This number is given for wbl(wait between lines)  $\leq$  2. For wbl=n {n>2} the timing will be (n+2)T.
3. This number is given for wbl(wait between lines)  $\leq$  2. For wbl=n {n>2} the timing will be (n+2)T.
4. Wait Between Frames (WBF) is a programmable parameter.

T<sub>cy</sub> is the cycle time of the LCD clock (shift clock). T<sub>delay</sub> is a circuit delay that is specified in the AC electrical specifications. 1–16 lines is a time period that can vary between one scan line and 16, depending on how the LCD controller is programmed in the VPW field of the LCVCR. 0–1,023 lines is a time period that can vary between 0 and 1,023 scan lines in the WBF field of the LCVCR.

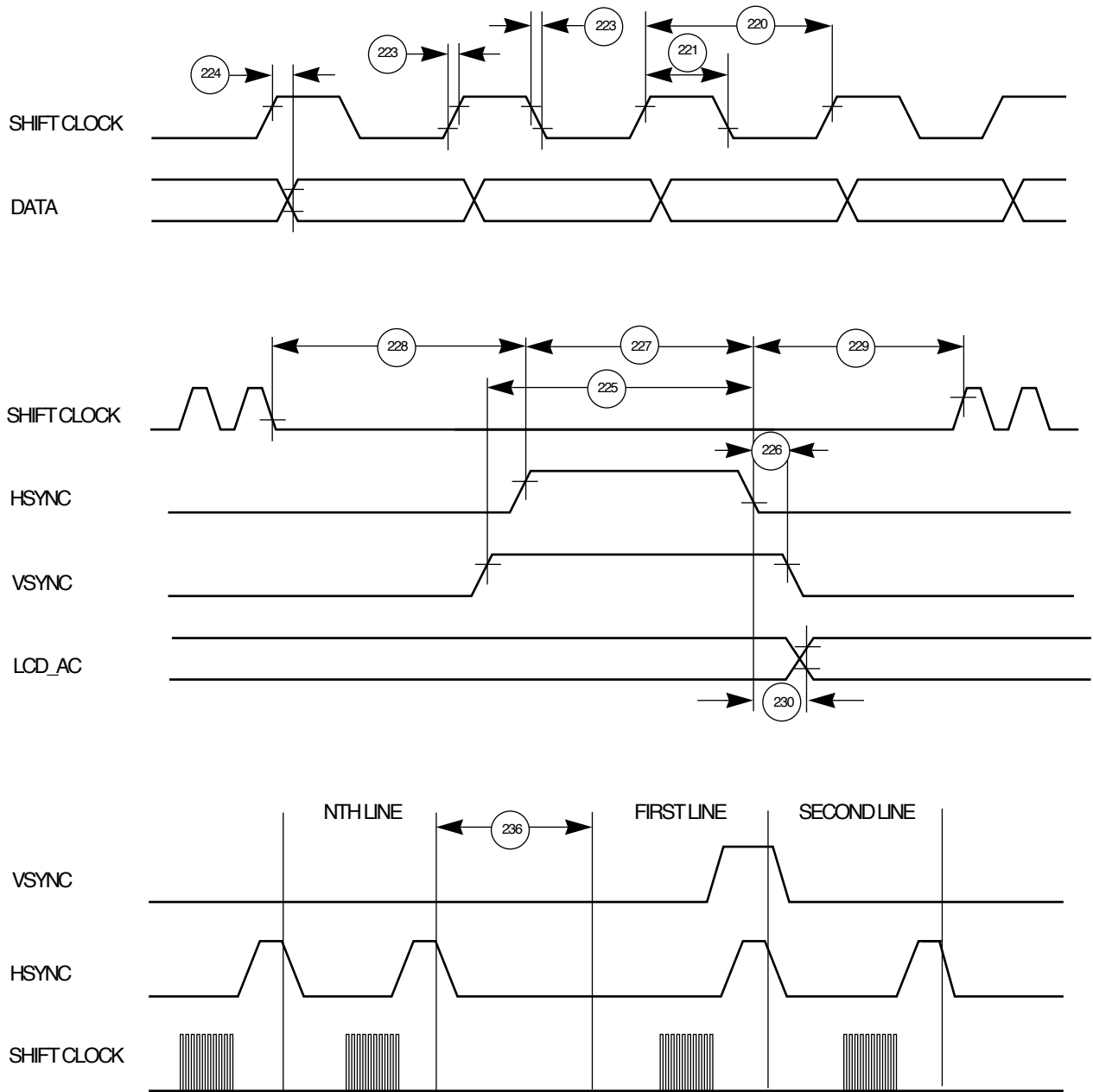


Figure 58. Passive Panel Timing Diagram

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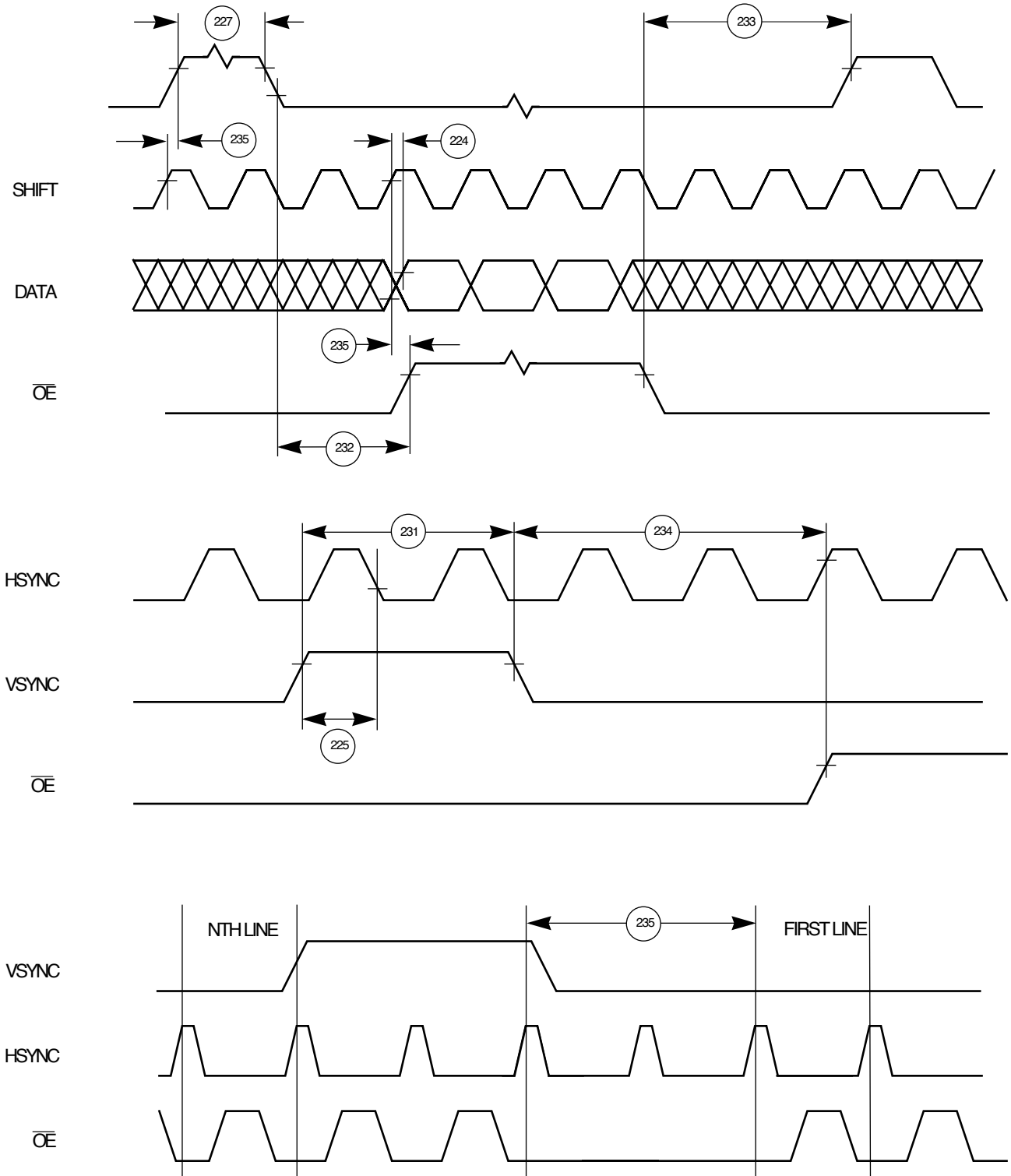


Figure 59. TFT Panel Timing Diagram

Table 22. Video Controller Timing

| NUM | CHARACTERISTIC                                  | 25MHZ |     | 40MHZ |     | 50MHZ |     | UNIT |
|-----|---|-------|-----|-------|-----|-------|-----|------|
|     |   | MIN   | MAX | MIN   | MAX | MIN   | MAX |      |
| 240 | Clock cycle time                                | 32    | —   | 32    | —   | 32    | —   | nsec |
| 241 | Clock high time                                 | 13    | —   | 13    | —   | 13    | —   | nsec |
| 242 | CLK/HSYNC/VSYNC/BLANK/FIELD rise and fall times | —     | 10  | —     | 10  | —     | 10  | nsec |
| 243 | Clock high to data valid                        | 10    | 25  | 10    | 25  | 10    | 25  | nsec |

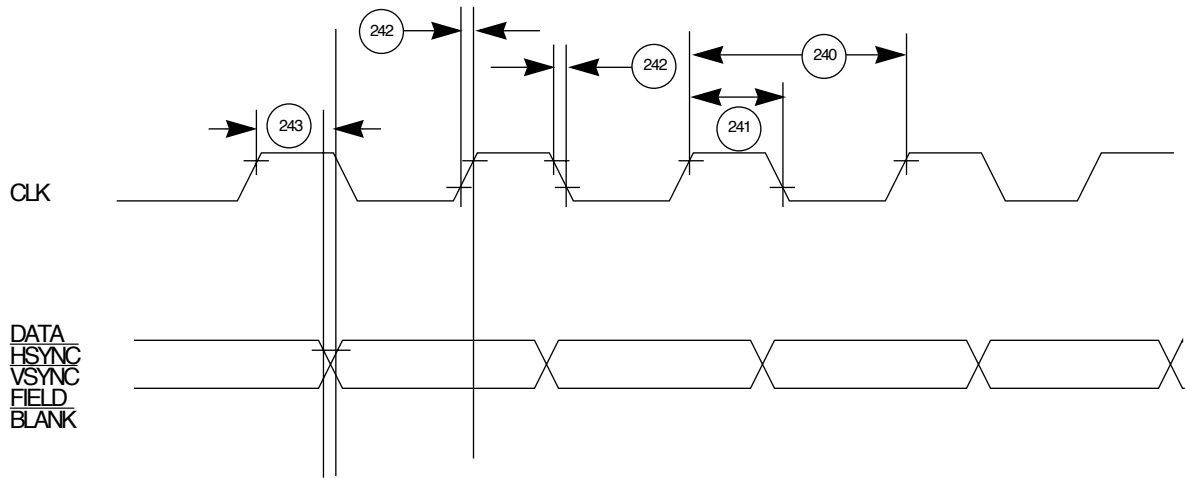


Figure 60. Video Controller Timing



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