SPECTRUM DIGITAL INCORPORATED

# TMS320VC5510 DSK

# Technical Reference

2002 DSP Development Systems

# TMS320VC5510 DSK
# Technical Reference

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# Contents

## About This Manual

This document describes the board level operations of the TMS320VC5510 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320VC5510 Digital Signal Processor.

The TMS320VC5510 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5510 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

## Notational Conventions

This document uses the following conventions.

The TMS320VC5510 will sometimes be referred to as the C55XX.

The TMS320VC5510 DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

*equations*
*!rd = !strobe&rw;*

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This book may contain cautions.
***This is an example of a caution statement.***
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

**Table 1: Hardware History**

| Revision | History |
|---|---|
| A | Alpha Release |
| B | Beta Release |
| C | Production Release |

**Table 2: Manual History**

| Revision | History |
|---|---|
| A | Alpha Release |
| B | Beta Release |
| C | Production Release |

# Chapter 1

# Introduction to the TMS320VC5510 DSK

Chapter One provides a description of the TMS320VC5510 DSK along with the key features and a block diagram of the circuit board.

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## 1.0 Key Features

The 5510 DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The DSK also serves as a hardware reference design for the TMS320VC5510 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

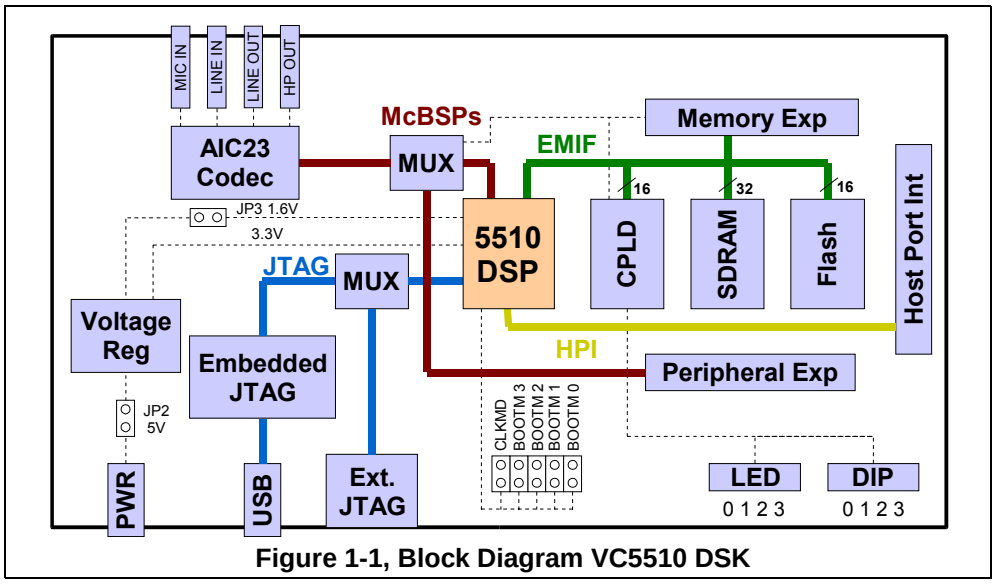


**Figure 1-1, Block Diagram VC5510 DSK**

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments 5510 DSP operating at 200MHz
- An AIC23 stereo codec
- 8 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Jumper selectable boot options
- Standard expansion connectors for daughter card use
- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+5V)

## 1.2 Functional Overview of the TMS320VC5510 DSK

The DSP interfaces to external SDRAM, Flash memory and an expansion memory interface connector through its 32-bit External Memory Interface (EMIF). The SDRAM accesses are in 32-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. McBSP1 is used for the codec control interface and McBSP2 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP1 and McBSP2 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board voltage regulators provide the 1.6V DSP core voltage, 3.3V digital and 3.3V analog voltages. A voltage supervisor monitors the internally generated voltage, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external JTAG connector.

### 1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

1) Connect the included power supply to the DSK.

2) Connect the DSK to your PC with a standard USB cable (also included).

3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file. You can access the help file through Code Composer's help menu. It can also be launched directly by double-clicking on the file c5510dsk.hlp in Code Composer's docs\hlp subdirectory.

### 1.4 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5510 is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 22 address bits are driven on the EMIF as address lines while the top 2 are decoded and driven as the chip enable for that particular region.

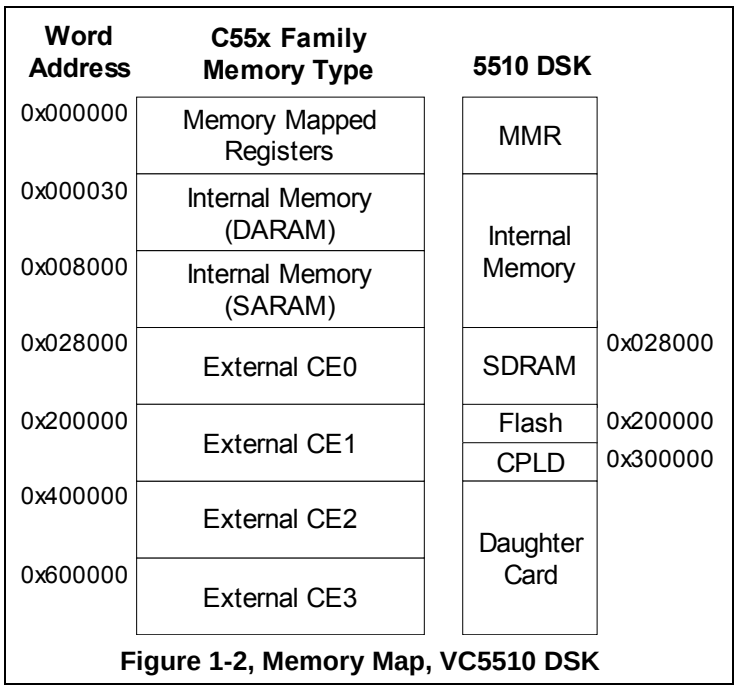


**Figure 1-2, Memory Map, VC5510 DSK**

The figure above shows a generic memory space map for a C55x family processor and a second mad specific to the components on a 5510 DSK. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the top half and the CPLD in the bottom half.

Internal memory on the 5510 starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM and a larger amount of internal SARAM. DARAM stands for Dual-Access RAM and is differentiated from SARAM (Single-Access RAM) in that two concurrent memory operations can be performed on the same block rather than one.

Internal memory is divided into 4Kword blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. DARAM blocks are the most precious because their dual-ported nature allows a higher rate of operation. There are 8 DARAM blocks and 32 SARAM blocks on a 5510 for a total of 160Kwords of internal memory.

### 1.5 Jumper Settings

The 5510 DSK has 5 on-board jumpers that define the DSP's boot configuration and reset state. The figure below shows these jumpers.

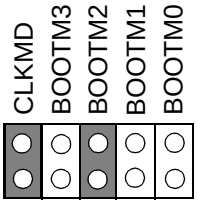


**Figure 1-3, JP4, DSP Boot Configuration - Default Setting**

The jumpers drive signals that directly correspond to the input on one of the DSP's configuration pins. If the jumper is on, the signal is driven to a logic 0. If the jumper is off, the signal is driven to a logic 1.

The CLKMD jumper configures the initial value of the CLKMD register. If the jumper is on, the initial CLKMD value is 0x2002 which implies that the PLL is disabled and the system clock runs at the frequency of the external reference (24MHz). If the jumper is off, the CLKMD value is 0x2006 and the system runs at half of the external reference (12MHz).

The 5510 has a number of boot modes that are selected at reset by sampling the BOOTM[3-0] pins. These pins can be configured with the on-board jumpers.

The 5510 can boot from asynchronous memory mapped in CE1 (Flash on the 5510 DSK board), serial EEPROM's connected to McBSP0 or a standard serial port on McBSP0. To boot from a particular device you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumpers and power cycle the board, the 5510 will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5510 usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins. In the special case where BOOTM[3:0] are all 0, the internal ROM is not active and execution will begin from external memory at the reset vector (0xFFFF00).

**Table 1: VC5510 DSK Boot Load Options**

| BOOTM[3:0] | BOOT PROCESS | EXECUTION START BYTE ADDRESS AFTER BOOT IS COMPLETE |
|---|---|---|
| 0000 | No Boot | FFFF00h (reset vector) |
| 0001 | Serial SPI EPROM boot from McBSP0 supporting 24 bit addressing | Destination specified in the boot table |
| 0010 | Reserved | - |
| 0011 | Reserved | - |
| 0010 | Reserved | - |
| 0101 | Reserved | - |
| 0110 | Reserved | - |
| 0111 | Reserved | - |
| 1000 | No boot | FFFF00h (reset vector) |
| 1001 | Serial SPI EPROM boot from McBSP0 supporting 16 bit addressing | Destination specified in the boot table |
| 1010 | Parallel EMIF boot from 8-bit asychronous memory | Destination specified in the boot table |
| **1011 *** | Parallel EMIF boot from 16-bit asychronous memory | Destination specified in the boot table |
| 1100 | Parallel EMIF boot from 32-bit asychronous memory | Destination specified in the boot table |
| 1101 | EHPI boot | 010000h (on-chip SARAM) |
| 1110 | Standard serial boot from McBSP0, 16-bit element length | Destination specified in the boot table |
| 1111 | Standard serial boot from McBSP0, 8-bit element length | Destination specified in the boot table |

Note: Jumper On = Logical 0
Jumper Off = Logical 1

***** Default Boot Load Option for DSK

### 1.6 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.6V and +3.3V using a dual voltage regulator. The +1.6V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug.

The core voltage on the DSK is selectable based on the output of GPIO0. If GPIO0 is high or configured as an input the core voltage will remain at +1.6V. If GPIO0 is driven low the voltage will drop to +1.1V.

There are two power test points on the DSK at JP2 and JP3. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. Normally these jumpers are both closed. To measure the current passing through remove the jumpers and connect the pins with a current measuring device.

The DSK also provides a separate +3.3V, 1A supply for the daughter card. The +3.3V supply is derived from the +5V power source with a separate linear regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector is used.

# Chapter 2

# Board Components

This chapter describes the operation of the major board components on the TMS320VC5510 DSK.

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## 2.1 CPLD (Programmable Logic)

The 'C5510 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 4 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

### 2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5510 can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the DSK, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the DSK on the installation CD-ROM.

### 2.1.2 CPLD Registers

The 4 CPLD memory-mapped registers allows users to control CPLD functions in software. On the 5510 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into the EMIF data space at word address 0x300000, right in the middle of CE1. They appear as 16-bit registers with a simple 16-bit asynchronous memory interface, although only the lower 8-bits are valid. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 4 registers in CPLD.

**Table 1: CPLD Register Definitions**

| Offset | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | USER_REG | USR_SW3<br>R | USR_SW2<br>R | USR_SW1<br>R | USR_SW0<br>R | USR_LED3<br>R/W<br>0(Off) | USR_LED2<br>R/W<br>0(Off) | USR_LED1<br>R/W<br>0(Off) | USR_LED0<br>R/W<br>0(Off) |
| 1 | DC_REG | DC_DET<br>R | 0 | DC_STAT1<br>R | DC_STAT0<br>R | DC_RST<br>R<br>0(No reset) | 0 | DC_CNTL1<br>R/W<br>0(low) | DC_CNTL0<br>R/W<br>0(low) |
| 4 | VERSION | CPLD_VER[3.0]<br>R | | | | 0 | BOARD VERSION[2.0]<br>R | | |
| 6 | MISC | 0 | 0 | VCORE_STAT<br>R | VCORE_MON<br>R/W<br>0<br>(Vcore Monitor Enabled) | TIN1<br>IN/OUT<br>R/W<br>(0 INPUT) | TIN0<br>IN/OUT<br>R/W<br>(0 INPUT) | McBSP2<br>ON/OFF<br>Board<br>R/W<br>0<br>(Onboard) | McBSP1<br>ON/OFF<br>Board<br>R/W<br>0<br>(Onboard) |

### 2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

**Table 2: CPLD USER_REG Register**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | USER_SW3 | R | User DIP Switch 3(1 = Off, 0 = On) |
| 6 | USER_SW2 | R | User DIP Switch 2(1 = Off, 0 = On) |
| 5 | USER_SW1 | R | User DIP Switch 1(1 = Off, 0 = On) |
| 4 | USER_SW0 | R | User DIP Switch 0(1 = Off, 0 = On) |
| 3 | USER_LED3 | R/W | User-defined LED 3 Control (0 = Off, 1 = On) |
| 2 | USER_LED2 | R/W | User-defined LED 2 Control (0 = Off, 1 = On) |
| 1 | USER_LED1 | R/W | User-defined LED 1 Control (0 = Off, 1 = On) |
| 0 | USER_LED0 | R/W | User-defined LED 0 Control (0 = Off, 1 = On) |

### 2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

**Table 3: DC_REG Register**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | DC_DET | R | Daughter Card Detect (1= Board detected) |
| 6 | 0 | R | Always 0 |
| 5 | DC_STAT1 | R | Daughter Card Status 1 (0=Low, 1 = High) |
| 4 | DC_STAT0 | R | Daughter Card Status 0 (0=Low, 1 = High) |
| 3 | DC_RST | R/W | Daughter Card Reset (0=No Reset, 1 = Reset) |
| 2 | 0 | R | Always zero |
| 1 | DC_CNTL1 | R/W | Daughter Card Control 1(0 = Low, 1 = High) |
| 0 | DC_CNTL0 | R/W | Daughter Card Control 0(0 = Low, 1 = High) |

### 2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

**Table 4: Version Register Bit Definitions**

| Bit # | Name | R/W | Description |
|---|---|---|---|
| 7 | CPLD_VER3 | R | Most Significant CPLD Version Bit |
| 6 | CPLD_VER2 | R | CPLD Version Bit |
| 5 | CPLD_VER1 | R | CPLD Version Bit |
| 4 | CPLD_VER0 | R | Least Significant CPLD Version Bit |
| 3 | 0 | R | Always 0 |
| 2 | DSK_VER2 | R | Most Significant DSK Board Version Bit |
| 1 | DSK_VER1 | R | DSK Board Version Bit |
| 0 | DSK_VER0 | R | Least Significant DSK Board Version Bit |

### 2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5510 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 and TIN1 bits are used to select whether the DSP's TIN0 and TIN1 (timer) signals are connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

The power supply logic monitors the core voltage for the DSP and supplies a power good signal that signifies that the core voltage is within an acceptable range. The power good signal can be read on the VCORE_STAT. If the signal is high, VCORE_STAT will read 1 indicating that the voltage is within range. A VCORE_STAT value of 0 indicates the voltage is outside of the normal operating range. The DSP reset circuit uses the power good signal to hold the DSP in reset when power is first applied as well as when any unexpected voltage glitches are encountered.

In certain circumstances (such as when transitioning back and forth between normal and low voltage mode) it is desirable to temporarily disable the power monitor's ability to reset the reset the DSP. A VCORE_MON setting of 1 keeps the DSP from being reset when the voltage changes. A VCORE_MON setting of 0 (default) leaves the reset capability enabled.

McBSP1SEL and McBSP2SEL control the McBSP1 and McBSP2. Usually these ports are used as the control and data ports of the on-board AIC23 codec. The power-on state of these bits (both 0s) represents that situation. Setting the corresponding bit to 1 enables the McBSP to the expansion daughter-card instead interface.

**Table 5: MISC Register**

| Bit | Name | R/W | Description |
|---|---|---|---|
| 7 | 0 | R | Always 0 |
| 6 | 0 | R | Always 0 |
| 5 | VCORE_STAT | R | Core power good indicator (0=power bad, 1= power good) |
| 4 | VCORE_MON0 | R/W | Vcore voltage monitor disable (0=enabled, 1= disabled) |
| 3 | TIN1SEL | R/W | TIN1 in/out on daughter card (0 = input, 1 = output) |
| 2 | TINSEL0 | R/W | TIN0 in/out on daughter card (0 = input, 1 = output) |
| 1 | MCBSP2SEL | R/W | McBSP2 on/off board (0 = on-board, 1 = off-board) |
| 0 | MCBSP1SEL | R/W | McBSP1 on/off board (0 = on-board, 1 = off-board) |

## 2.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. McBSP1 is used as the unidirectional control channel. It should be programmed to send a 16-bit control word to the AIC23 in SPI format. The top 7 bits of the control word should specify the register to be modified and the lower 9 should contain the register value. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP2 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5510 DSK.

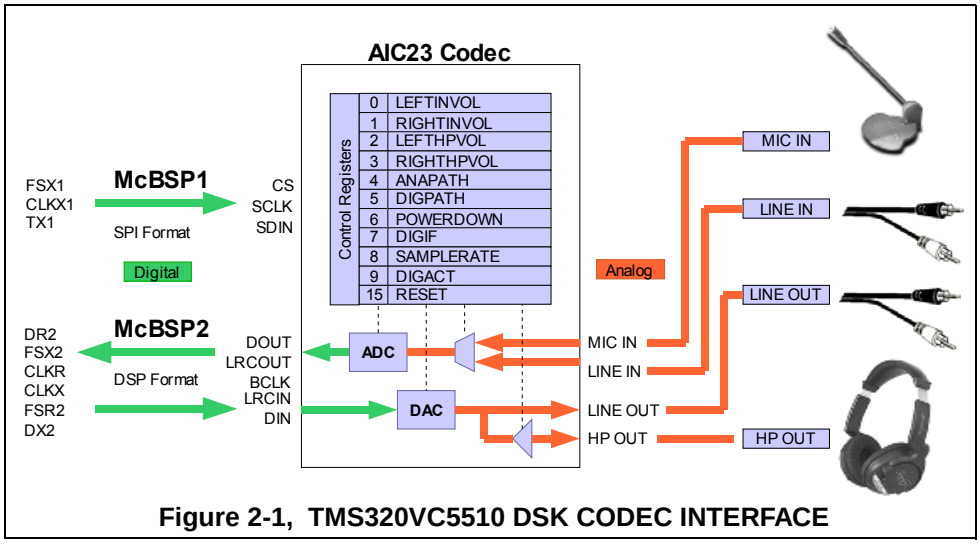



**Figure 2-1, TMS320VC5510 DSK CODEC INTERFACE**

### 2.3 Synchronous DRAM

The DSK uses an industry standard 64 megabit Synchronous SDRAM. It uses a 32-bit interface and is used with a 100MHz external memory clock. Since the DSP runs at 200MHz, the EMIF must be programmed to use the SDRAM at half the core clock rate.

The SDRAM occupies both chip enable 0 and 1. It appears on both chip enables because it is twice the size of a single chip enable space. Since the Flash and CPLD use chip enable 1, the DSK examples configure CE1 as asynchronous memory for their use and the SDRAM on CE1 is invisible.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

### 2.4 Flash Memory

The DSK provides 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M x 16 parts. The Flash is mapped into CE1 space because that is where the 16-bit asychronous bootloader looks for a boot image when booting from the Flash. The space is shared by the CPLD, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 80ns.

### 2.5 LEDs and DIP Switches

The DSK includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

### 2.6 Daughter Card Interface

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as McBSP2.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The DSK also multiplexes the McBSP1 and McBSP2 of on-board or external use. This function is controlled through the CPLD MISC register.

The timer signals on the peripheral expansion connector have connections for both inputs and outputs. since the VC5510 does not have separate timer inputs and outputs, the CPLD is used to select whether the input or output pin should be connected to the timer. This selection is also controlled through the CPLD MISC register.

# Chapter 3

# Physical Description

This chapter describes the physical layout of the TMS320VC5510 DSK and its connectors.

**Topic** **Page**

### 3.1 Board Layout

The VC5510 DSK is a 8.25 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the VC5510 DSK.

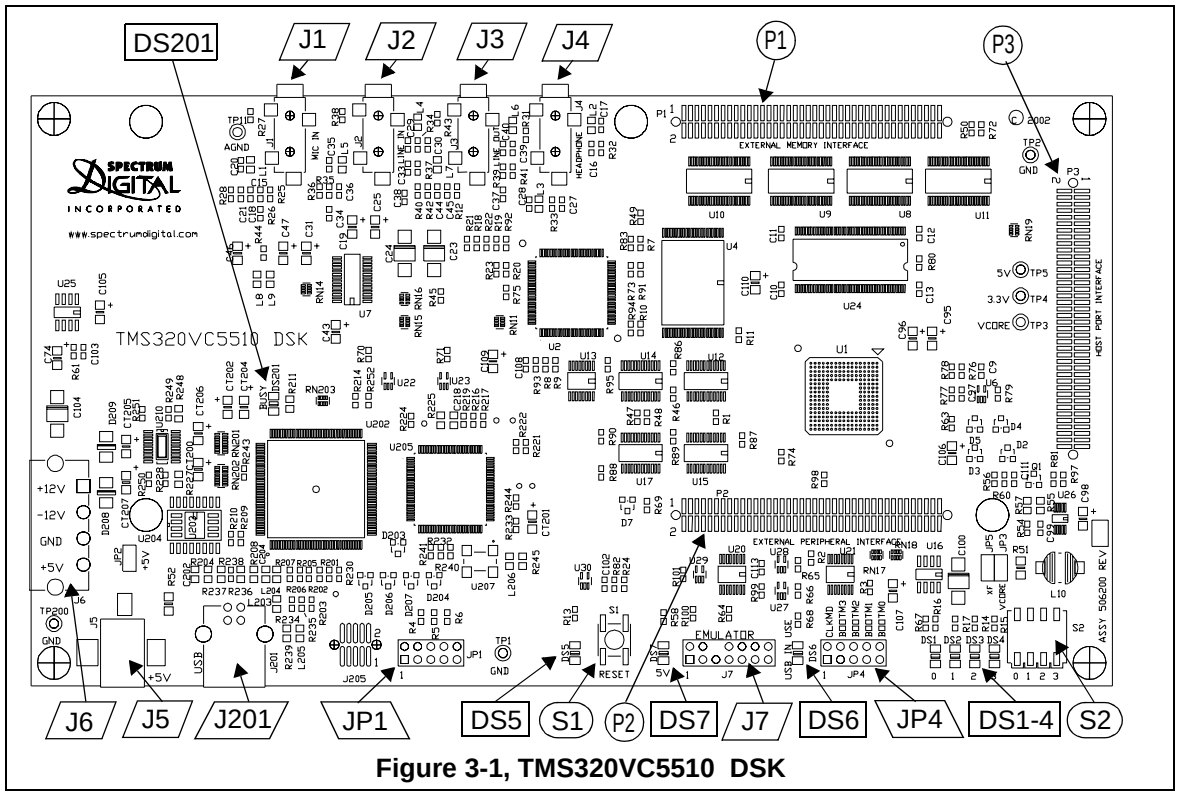



**Figure 3-1, TMS320VC5510 DSK**

## 3.2 Connector Index

The TMS320VC5510 DSK has many connectors which provide the user access to the various signals on the DSK.

**Table 1: TMS320VC5510 DSK Connectors**

| Connector | # Pins | Function |
|---|---|---|
| P1 | 80 | Memory |
| P2 | 80 | Peripheral |
| P3 | 80 | HPI |
| J1 | 2 | Microphone |
| J2 | 2 | Line In |
| J3 | 2 | Line Out |
| J4 | 2 | Speaker |
| J5 | 2 | +5 Volt |
| J6 * | 4 | Optional Power Connector |
| J7 | 14 | External JTAG |
| J201 | 5 | USB Port |
| JP1 | 10 | CPLD Programming |
| JP4 | 8 | DSP Configuration Jumper |

**Note:** "*****" Not populated

## 3.3 Expansion Connectors

The TMS320VC5510 DSK supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

The three expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

**Note: I** is on an Input pin
**O** is on an Output pin
**Z** is on a High Impedance pin

### 3.3.1 P1, Memory Expansion Connector

**Table 2: P1, Memory Expansion Connector**

| Pin # | Signal Name | I/O/Z | Pin # | Signal Name | I/O/Z |
|---|---|---|---|---|---|
| 1 | +5 Volts | O | 2 | +5 volts | O |
| 3 | A21 | O | 4 | A20 | O |
| 5 | A19 | O | 6 | A18 | O |
| 7 | A17 | O | 8 | A16 | O |
| 9 | A15 | O | 10 | A14 | O |
| 11 | GND | O | 12 | GND | O |
| 13 | A13 | O | 14 | A12 | O |
| 15 | A11 | O | 16 | A10 | O |
| 17 | A9 | O | 18 | A8 | O |
| 19 | A7 | O | 20 | A6 | O |
| 21 | +5 Volts | O | 22 | +5 Volts | O |
| 23 | A5 | O | 24 | A4 | O |
| 25 | A3 | O | 26 | A2 | O |
| 27 | BE3n | O | 28 | BE2n | O |
| 29 | BE1n | O | 30 | BE0n | O |
| 31 | GND | O | 32 | GND | O |
| 33 | D31 | I/O/Z | 34 | D30 | I/O/Z |
| 35 | D29 | I/O/Z | 36 | D28 | I/O/Z |
| 37 | D27 | I/O/Z | 38 | D26 | I/O/Z |
| 39 | D25 | I/O/Z | 40 | D24 | I/O/Z |
| 41 | +3.3 Volts | O | 42 | +3.3 Volts | O |
| 43 | D23 | I/O/Z | 44 | D22 | I/O/Z |
| 45 | D21 | I/O/Z | 46 | D20 | I/O/Z |
| 47 | D19 | I/O/Z | 48 | D18 | I/O/Z |
| 49 | D17 | I/O/Z | 50 | D16 | I/O/Z |
| 51 | GND | O | 52 | GND | O |
| 53 | D15 | I/O/Z | 54 | D14 | I/O/Z |
| 55 | D13 | I/O/Z | 56 | D12 | I/O/Z |
| 57 | D11 | I/O/Z | 58 | D10 | I/O/Z |
| 59 | D9 | I/O/Z | 60 | D8 | I/O/Z |
| 61 | GND | O | 62 | GND | O |
| 63 | D7 | I/O/Z | 64 | D6 | I/O/Z |
| 65 | D5 | I/O/Z | 66 | D4 | I/O/Z |
| 67 | D3 | I/O/Z | 68 | D2 | I/O/Z |
| 69 | D1 | O | 70 | D0 | O |
| 71 | GND | O | 72 | GND | O |
| 73 | REn | O | 74 | WEn | O |
| 75 | OEn | O | 76 | RDYn | I |
| 77 | CE3n | O | 78 | CE2n | O |
| 79 | GND | O | 80 | GND | O |

### 3.3.2 P2, Peripheral Expansion Connector

**Table 3: P2, Peripheral Expansion Connector**

| Pin # | Signal Name | I/O/Z | Pin # | Signal Name | I/O/Z |
|---|---|---|---|---|---|
| 1 | +12 Volts * | O | 2 | -12 Volts * | O |
| 3 | GND | O | 4 | GND | O |
| 5 | +5 Volts | O | 6 | +5 Volts | O |
| 7 | GND | O | 8 | GND | O |
| 9 | +5 Volts | O | 10 | +5 Volts | O |
| 11 | RESERVED | | 12 | RESERVED | |
| 13 | RESERVED | | 14 | RESERVED | |
| 15 | RESERVED | | 16 | RESERVED | |
| 17 | RESERVED | | 18 | RESERVED | |
| 19 | +3.3 Volts | O | 20 | +3.3 Volts | O |
| 21 | CLKX0 | I/O/Z | 22 | RESERVED | |
| 23 | FSX0 | I/O/Z | 24 | DX0 | O/Z |
| 25 | GND | O | 26 | GND | O |
| 27 | CLKR0 | I/O/Z | 28 | RESERVED | |
| 29 | FSR0 | I/O/Z | 30 | DR0 | I |
| 31 | GND | O | 32 | GND | O |
| 33 | CLKX1 | I/O/Z | 34 | CLKS1 | I |
| 35 | FSX1 | I/O/Z | 36 | DX1 | O/Z |
| 37 | GND | O | 38 | GND | O |
| 39 | CLKR1 | I/O/Z | 40 | RESERVED | |
| 41 | FSR1 | I/O/Z | 42 | DR1 | Z |
| 43 | GND | O | 44 | GND | O |
| 45 | TOUT0 | Z | 46 | TIN0 | I |
| 47 | INT0n | I | 48 | INT2n | I |
| 49 | TOUT1 | O | 50 | TIN1 | I |
| 51 | GND | O | 52 | GND | O |
| 53 | INT1n | I | 54 | IACKn | I |
| 55 | RESERVED | | 56 | IOSTRBn | O |
| 57 | RESERVED | | 58 | INT4n | I |
| 59 | RESETn | O | 60 | RESERVED | |
| 61 | GND | O | 62 | GND | O |
| 63 | DC_CNTL1 | O | 64 | DC_CNTL0 | O |
| 65 | DC_STAT1 | I | 66 | DC_STAT0 | I |
| 67 | INT3n | I | 68 | RESERVED | |
| 69 | RESERVED | | 70 | RESERVED | |
| 71 | RESERVED | | 72 | RESERVED | |
| 73 | RESERVED | | 74 | RESERVED | |
| 75 | DETECTn | I | 76 | GND | O |
| 77 | GND | O | 78 | CLKOUT | O |
| 79 | GND | O | 80 | GND | O |

### 3.3.3 P3, HPI Expansion Connector

**Table 4: P3, HPI Expansion Connector**

| Pin # | Signal Name | I/O/Z | Pin # | Signal Name | I/O/Z |
|---|---|---|---|---|---|
| 1 | +5 Volts | O | 2 | +5 Volts | O |
| 3 | CLKX2 | I/O/Z | 4 | CLKR2 | I/O/Z |
| 5 | FSX2 | I/O/Z | 6 | FSR2 | I/O/Z |
| 7 | DX2 | O/Z | 8 | DR2 | I |
| 9 | IO4 | I/O | 10 | CLKS2 | I |
| 11 | GND | O | 12 | GND | O |
| 13 | HRW | I | 14 | HCNTL0 | I |
| 15 | HMODE | I | 16 | HCS | I |
| 17 | IO6 | I/O | 18 | IO7 | I/O |
| 19 | HDS2 | I | 20 | HDS1 | I |
| 21 | +5 Volts | O | 22 | +5 Volts | O |
| 23 | HRDY | O/Z | 24 | HINT | O/Z |
| 25 | HA19 | I | 26 | HA18 | I |
| 27 | HA17 | I | 28 | HA16 | I |
| 29 | HBE1 | I | 30 | HBE0 | I |
| 31 | GND | O | 32 | GND | O |
| 33 | HA15 | I | 34 | HA14 | I |
| 35 | HA13 | I | 36 | HA12 | I |
| 37 | HA11 | I | 38 | HA10 | I |
| 39 | HA9 | I | 40 | HA8 | I |
| 41 | +5 Volts | O | 42 | +5 Volts | O |
| 43 | HA7 | I | 44 | HA6 | I |
| 45 | HA5 | I | 46 | HA4 | I |
| 47 | HA3 | I | 48 | HA2 | I |
| 49 | HA1 | I | 50 | HA0 | I |
| 51 | GND | O | 52 | GND | O |
| 53 | HD15 | I/O/Z | 54 | HD14 | I/O/Z |
| 55 | HD13 | I/O/Z | 56 | HD12 | I/O/Z |
| 57 | HD11 | I/O/Z | 58 | HD10 | I/O/Z |
| 59 | HD9 | I/O/Z | 60 | HD8 | I/O/Z |
| 61 | GND | O | 62 | GND | O |
| 63 | HD7 | I/O/Z | 64 | HD6 | I/O/Z |
| 65 | HD5 | I/O/Z | 66 | HD4 | I/O/Z |
| 67 | HD3 | I/O/Z | 68 | HD2 | I/O/Z |
| 69 | HD1 | I/O/Z | 70 | HD0 | I/O/Z |
| 71 | GND | O | 72 | GND | O |
| 73 | HOLDA | O/Z | 74 | HOLD | I |
| 75 | INT5n | I | 76 | IO5 | I/O |
| 77 | XF | O | 78 | HPI_RST | I |
| 79 | GND | O | 80 | GND | O |

### 3.4 Audio Connectors

The VC5510 DSK has 4 audio connectors. They are described in the following sections.

#### 3.4.1 J1, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

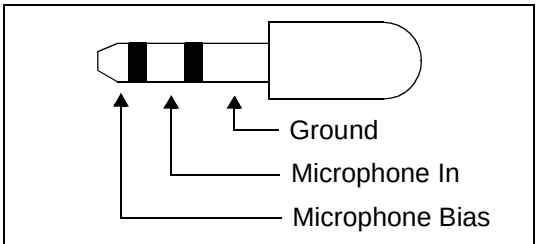



**Figure 3-2, Microphone Stereo Jack**

#### 3.4.2 J2, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

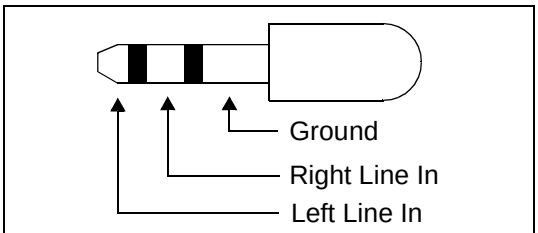



**Figure 3-3, Audio Line In Stereo Jack**

### 3.4.3 J3, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

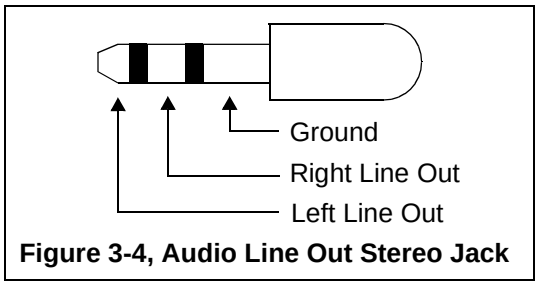



**Figure 3-4, Audio Line Out Stereo Jack**

### 3.4.4 J4, Headphone Connector

Connector J4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below

.

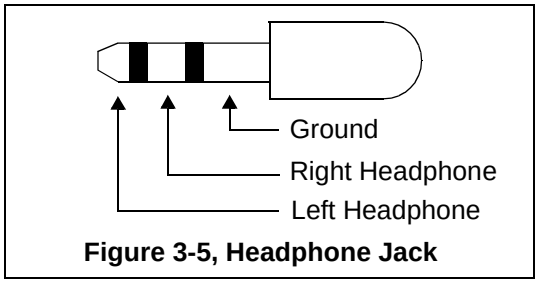



**Figure 3-5, Headphone Jack**

### 3.5 Power Connectors

The VC5510 DSK has 2 power connectors. They are described in the following sections.

#### 3.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320VC5510 DSK via the J5 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.

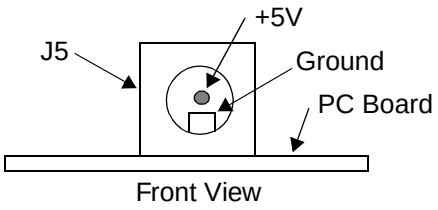



**Figure 3-6, TMS320VC5510 DSK Power Connector**

#### 3.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15-24-4041. The table below shows the voltages on the respective pins.

**Table 5: J6, Optional Power Connector**

| Pin # | Voltage Level |
|---|---|
| 1 | +12 Volts |
| 2 | -12 Volts |
| 3 | Ground |
| 4 | +5 Volts |

**WARNING !**
Do not plug into J5 and J6 at the same time.

### 3.6 Miscellaneous Connectors

The VC5510 DSK has 3 additional connectors to aid the user in developing with this product. They are described in the following sections.

#### 3.6.1 J201, USB Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

**Table 6: J201, USB Connector**

| Pin # | USB Signal Name |
|---|---|
| 1 | USBVdd |
| 2 | D+ |
| 3 | D- |
| 4 | USB Vss |
| 5 | Shield |
| 6 | Shield |

#### 3.6.2 J7, External JTAG Connector

The TMS320VC5510 DSK is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

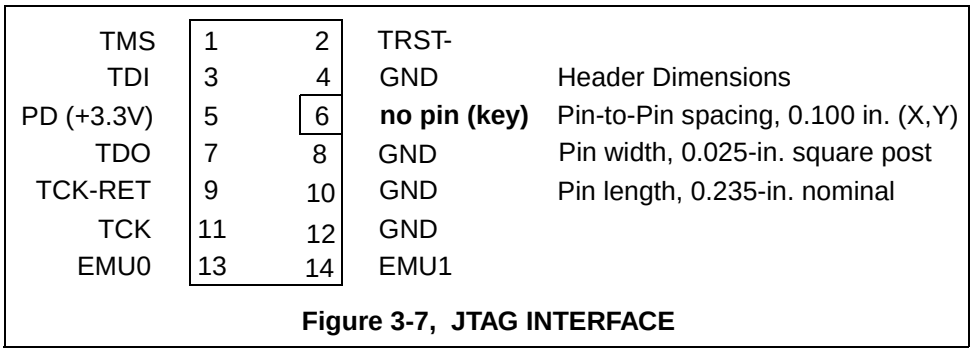



**Figure 3-7, JTAG INTERFACE**

The signal names for each pin are shown in the table below.

**Table 7: J7, JTAG Interface**

| Pin # | Signal Name |
|---|---|
| 1 | TMS |
| 2 | TRST- |
| 3 | TDI |
| 4 | GND |
| 5 | PD |
| 6 | no pin |
| 7 | TDO |
| 8 | GND |
| 9 | TCK-RET |
| 10 | GND |
| 11 | TCK |
| 12 | GND |
| 13 | EMU0 |
| 14 | EMU1 |

### 3.6.3 JP1, PLD Programming Connector

This connector interfaces to the Altera CPLD, U20. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

## 3.7 System LEDs

TheTMS320VC5510 DSK has four system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

**Table 8: System LEDs**

| Reference Designator | Color | Function | On Signal State |
|---|---|---|---|
| DS6 | Green | USB Emulation in use. When External JTAG Emulator is used this LED is off. | 1 |
| DS7 | Green | +5 Volt present | 1 |
| DS5 | Orange | RESET Active | 1 |
| DS201 | Green | USB Active, Blinks during USB data transfer | 1 |

### 3.8 Reset Switch

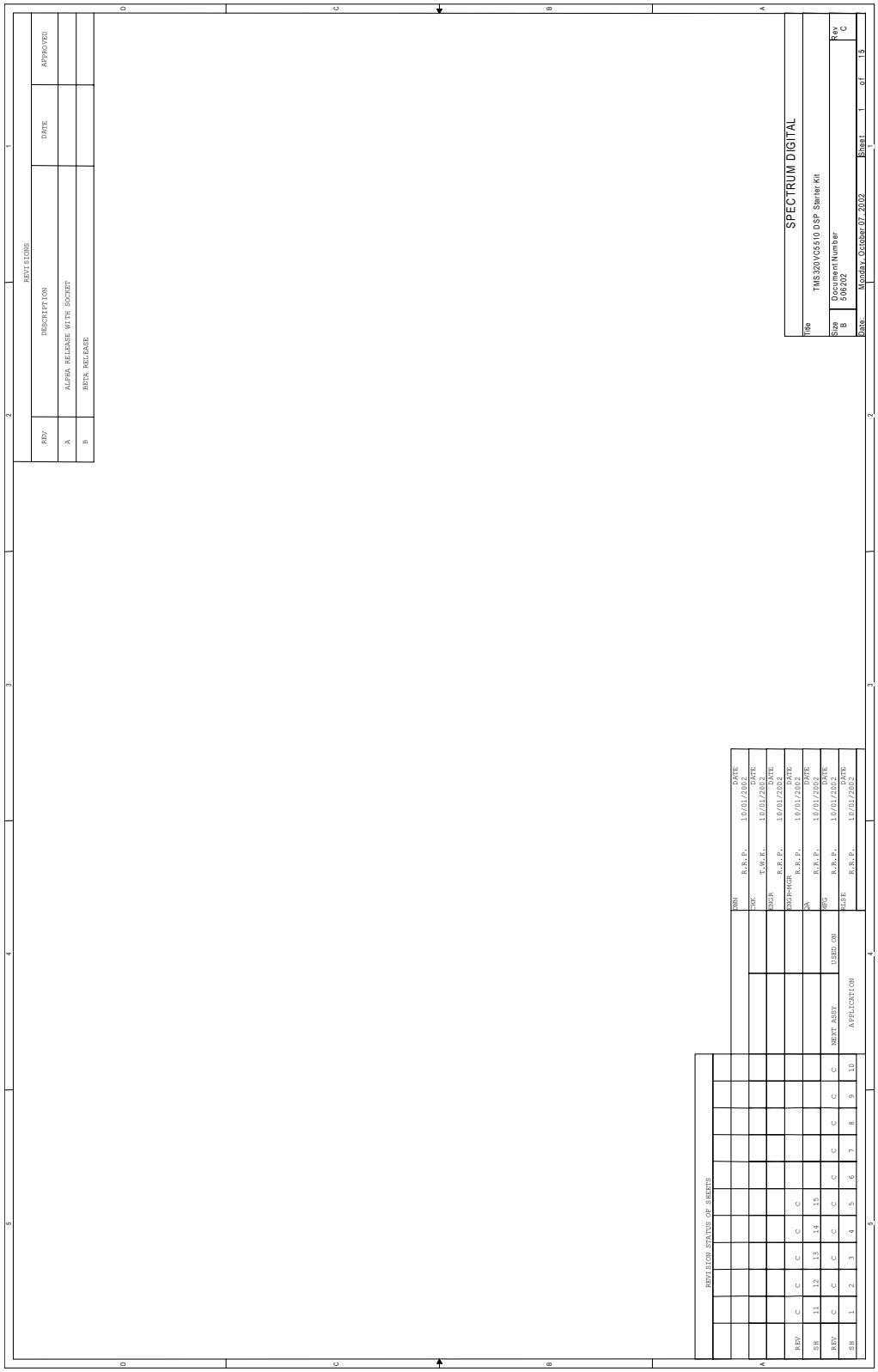
There are three resets on the TMS320VC5510 DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5510.

External sources which control the reset are push button S1, and the on board embedded USB JTAG emulator.

# Appendix A

# Schematics

This appendix contains the schematics for the TMS320VC5510 DSK. Board components with designators over 200 (e.g. DS210, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.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REV
DESCRIPTION
DATE
APPROVED
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ALPHA RELEASE WITH SOCKET
B
BETA RELEASE
SPECTRUM DIGITAL
Title
TMS320VC5510 DSP Starter Kit
Size
B
Document Number
506202
Rev
C
Date:
Monday, October 07, 2002
Sheet
1
of
15
DRAWN
R.R.P.
10/01/2102
CHK
T.W.K.
10/01/2102
ENGR
R.R.P.
10/01/2102
ENGR-MGR
R.R.P.
10/01/2102
QA
R.R.P.
10/01/2102
MFG
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RLSE
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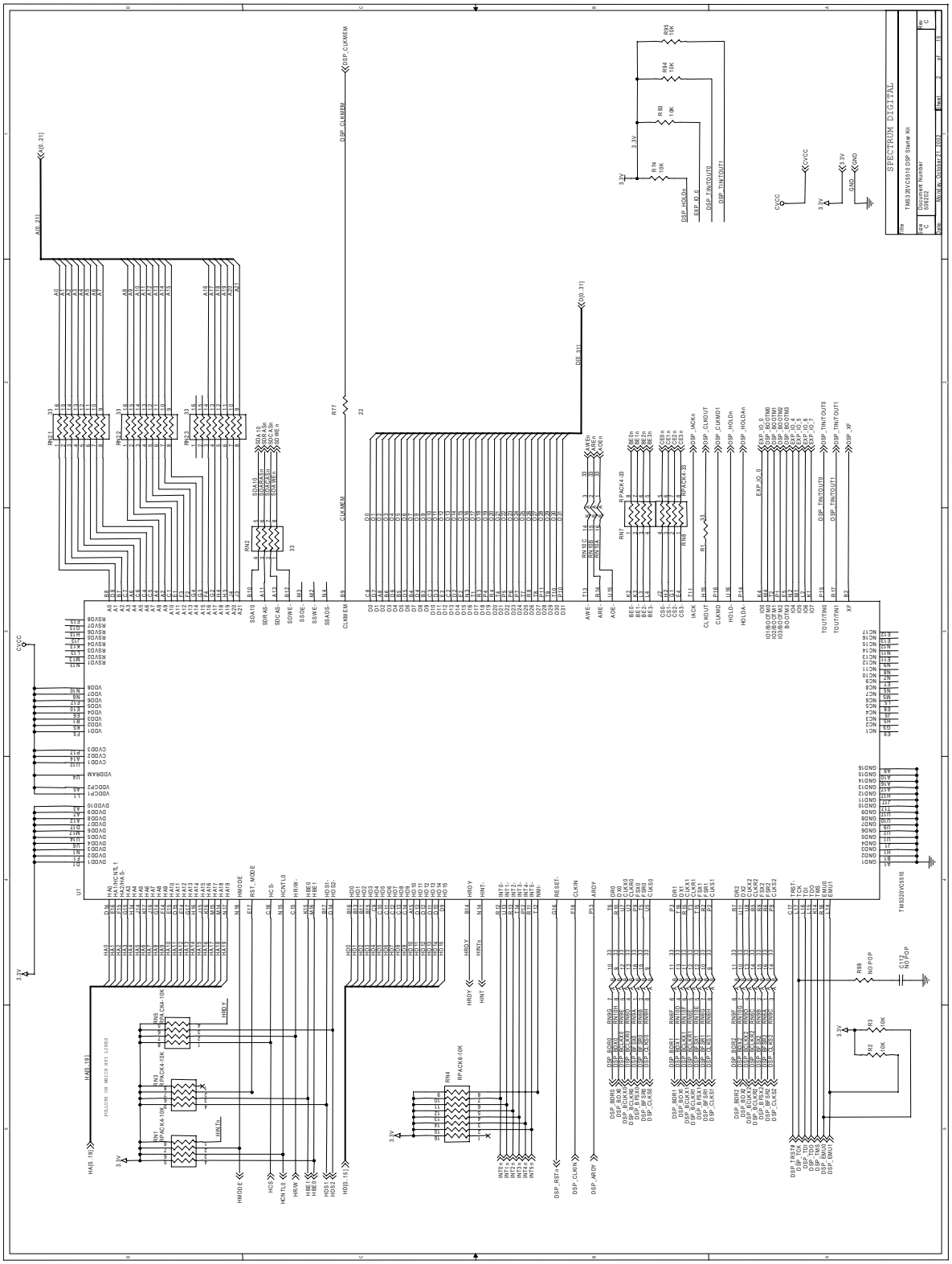
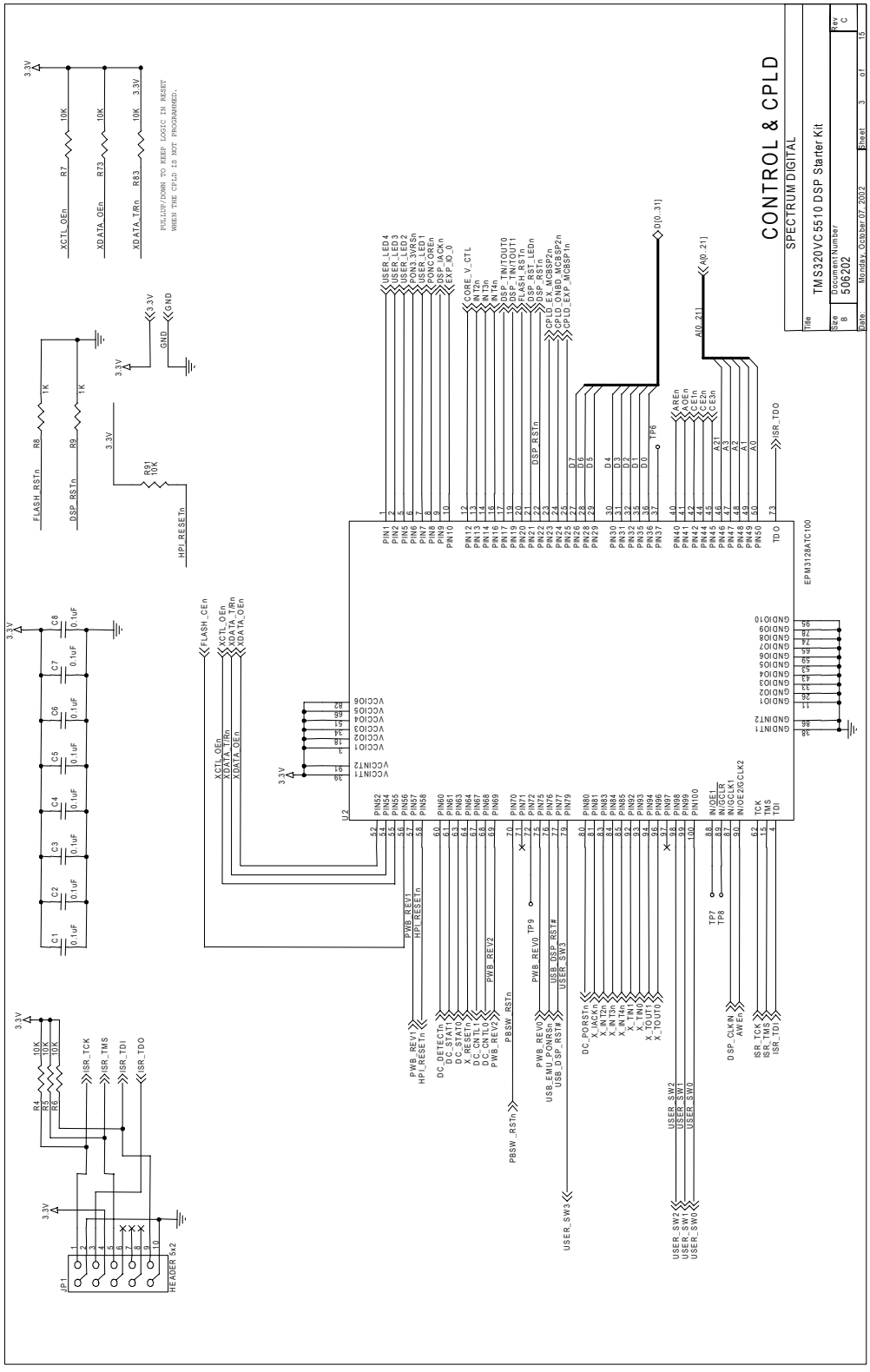
10/01/2102
DATE
REVISION STATUS OF SHEETS
NEXT ASSY
USED ON
APPLICATION




CONTROL & CPLD
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TMS320VC5510 DSP Starter Kit
Document Number
506202
Monday, October 07, 2002
Sheet 3 of 15
Rev C
Size B
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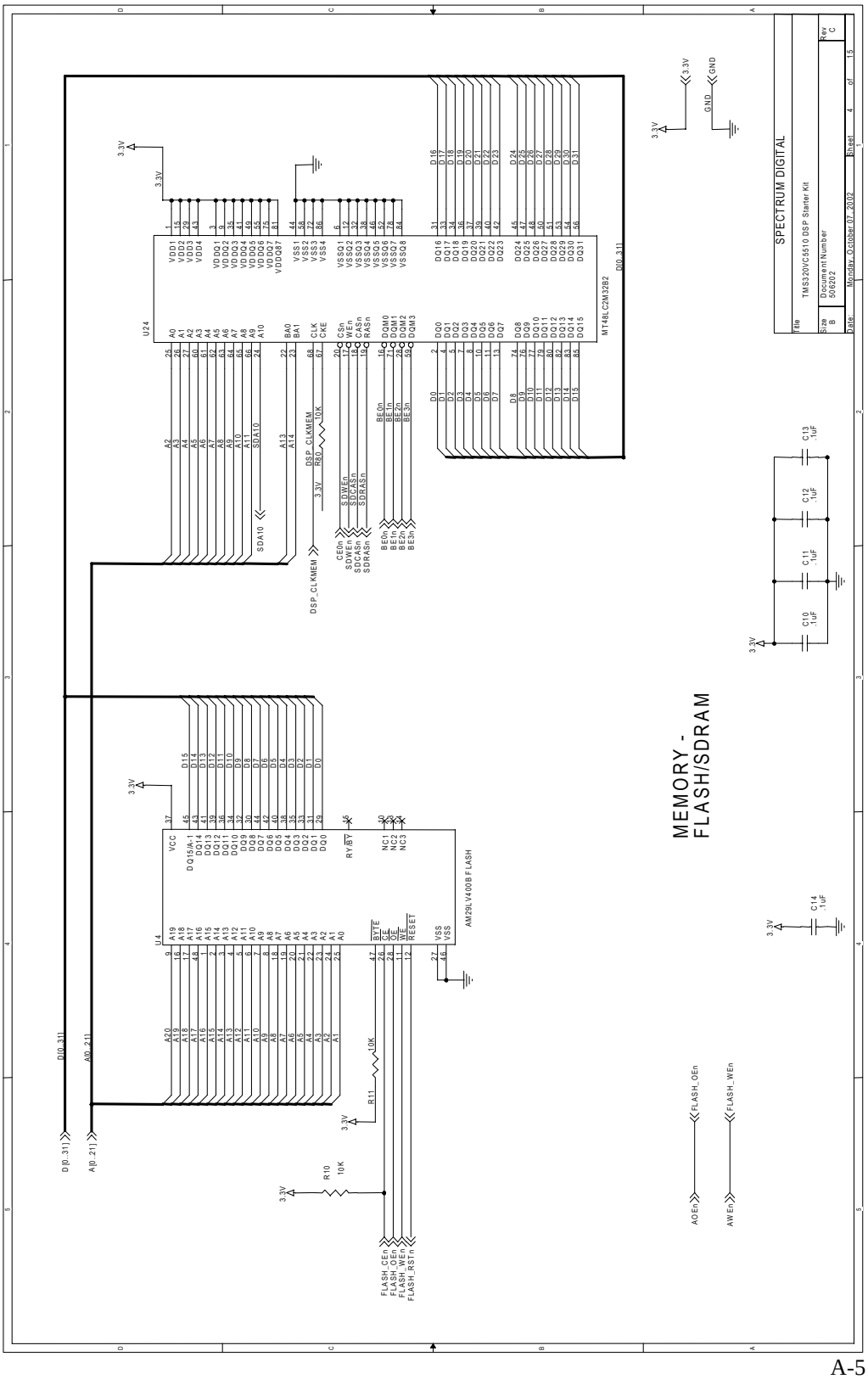
HEADER 5x2
PULLUP/DOWN TO KEEP LOGIC IN RESET
WHEN THE CPLD IS NOT PROGRAMMED.


MEMORY -
FLASH/SDRAM
SPECTRUM DIGITAL
TMS320VC5510 DSP Starter Kit
Document Number
505202
Monday, October 07, 2002
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MT48LC2M32B2
U4
AM29LV400B FLASH
DSP_CLKMEM
SDA10
SDWEn
SDCASn
SDRASn
FLASH_CEn
FLASH_OEn
FLASH_WEn
FLASH_RSTn
FLASH_OEn
FLASH_WEn
D[0..31]
A[0..21]
R10 10K
R11 10K
R60 10K
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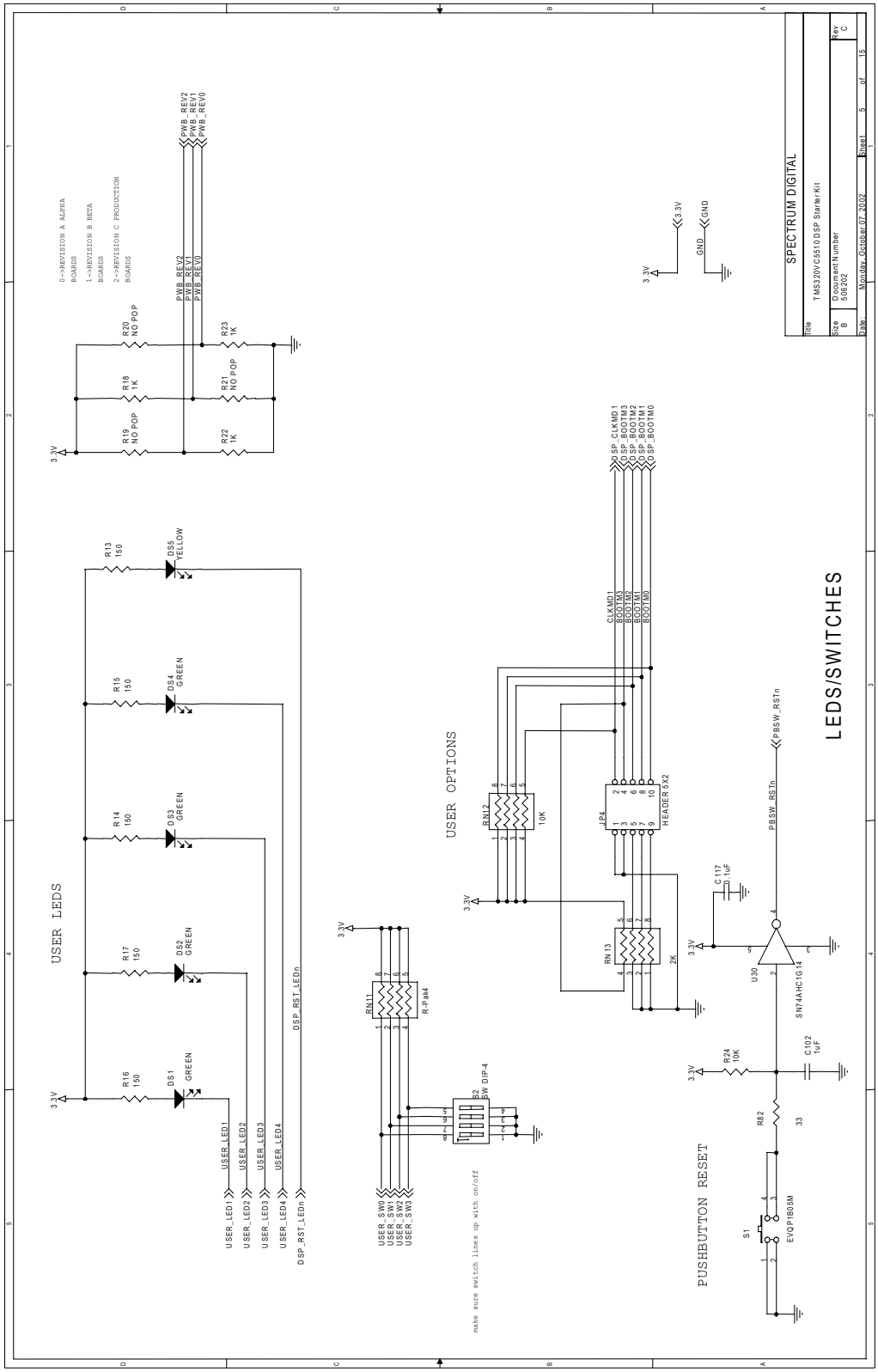
C11 1uF
C12 .1uF
C13 .1uF
C14 .1uF
3.3V
GND


LEDS/SWITCHES
USER LEDS
USER OPTIONS
PUSHBUTTON RESET
SPECTRUM DIGITAL
TMS320VC5510 DSP Starter Kit
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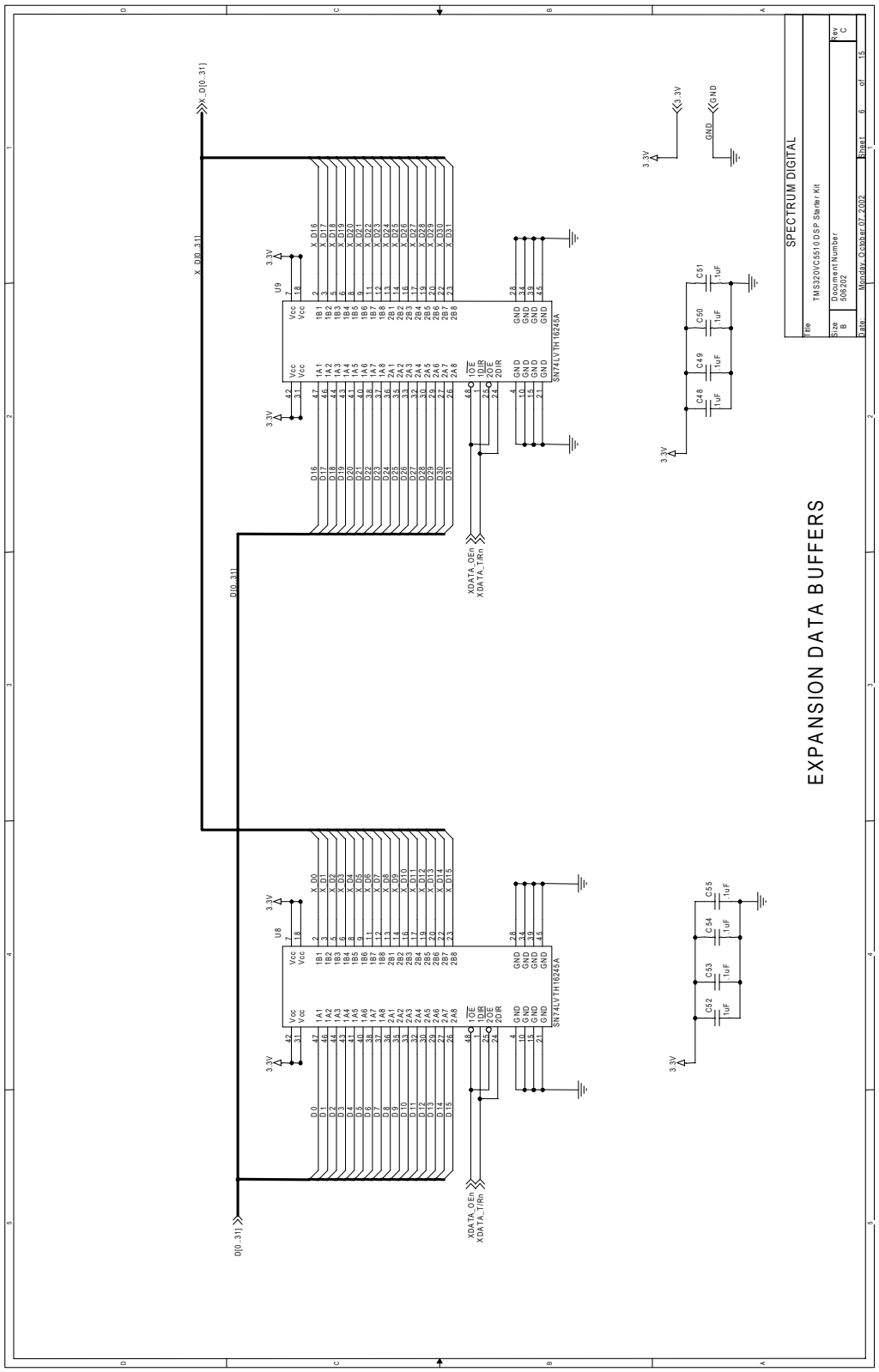
1->REVISION B BETA BOARDS
2->REVISION C PRODUCTION BOARDS
PWB_REV2
PWB_REV1
PWB_REV0
R20 NO POP
R23 1K
R18 1K
R21 NO POP
R19 NO POP
R22 1K
R13 150
R15 150
R14 150
R17 150
R16 150
DS5 YELLOW
DS4 GREEN
DS3 GREEN
DS2 GREEN
DS1 GREEN
USER_LED1
USER_LED2
USER_LED3
USER_LED4
DSP_RST_LEDn
RN12 10K
RN13 2K
RN11 R-Pak4
JP4 HEADER 5X2
CLKMD1
BOOTM3
BOOTM2
BOOTM1
BOOTM0
S2 SW DIP-4
USER_SW0
USER_SW1
USER_SW2
USER_SW3
make sure switch lines up with on/off
C117 0.1uF
C102 1uF
R24 10K
R82 33
S1 EVQP1B05M
U30 SN74AHC1G14
PBSW_RSTn
3.3V
GND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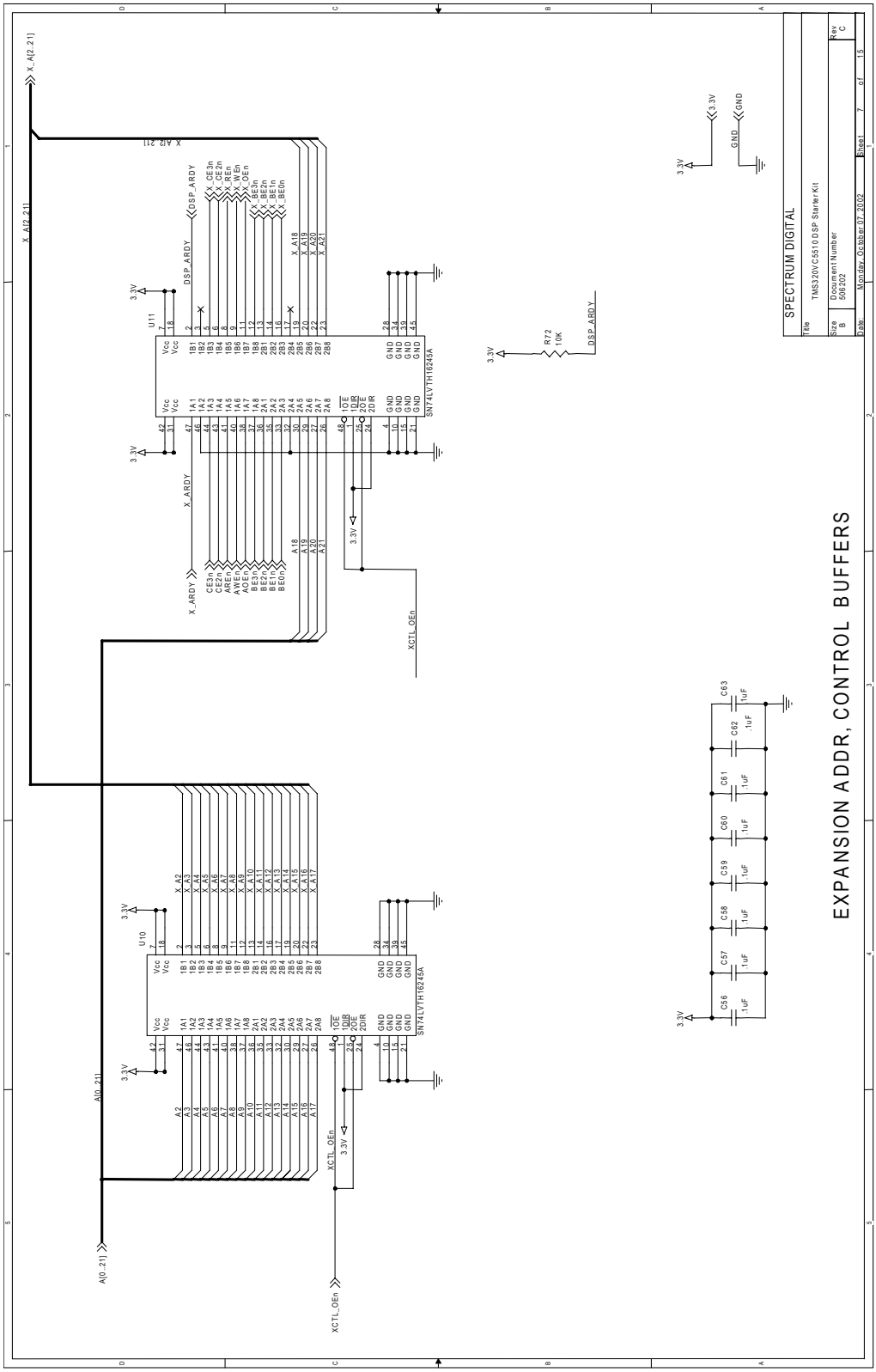
GND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C59
C60
C61
C62
C63
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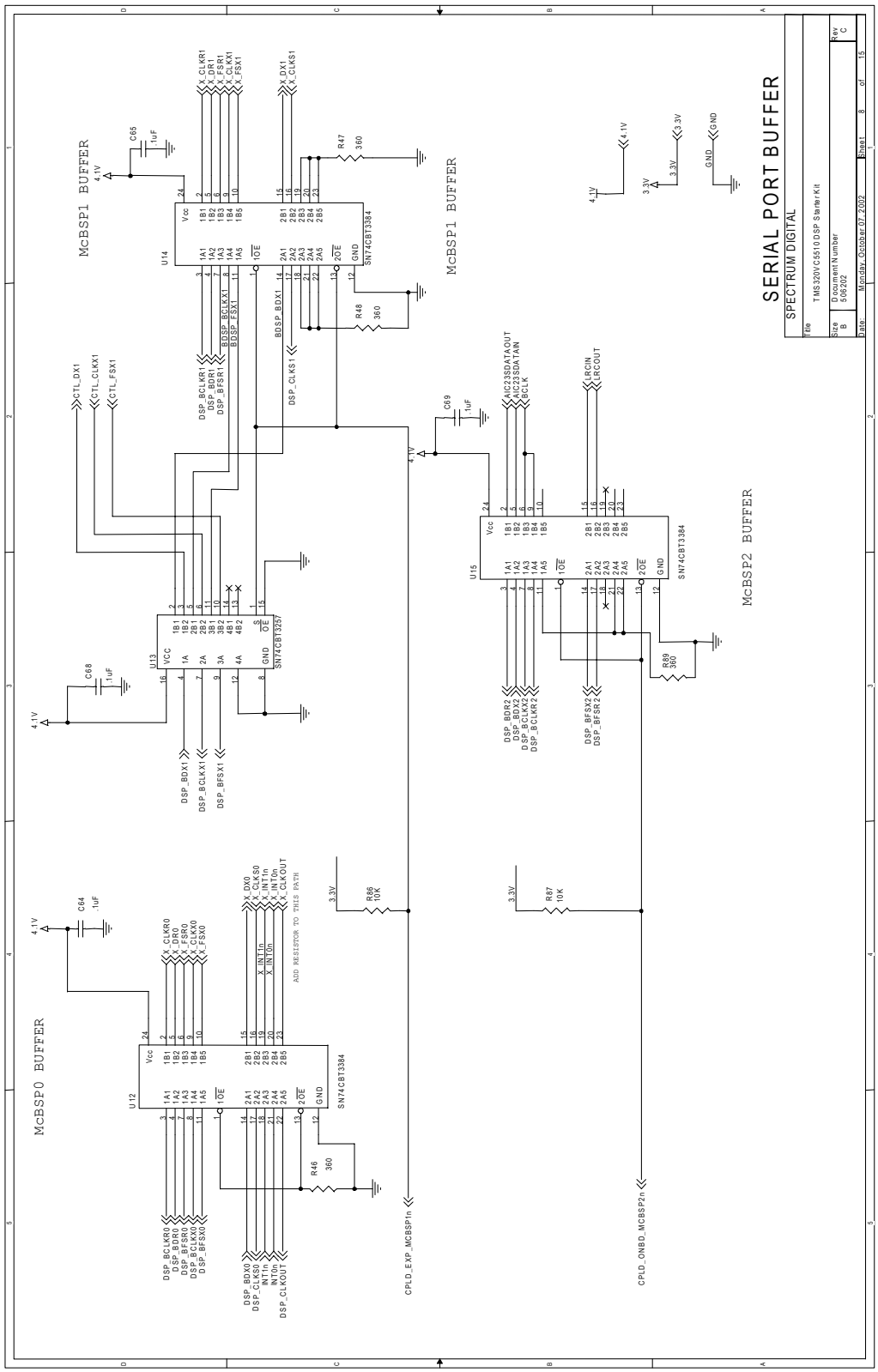
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McBSP1 BUFFER
McBSP1 BUFFER
McBSP2 BUFFER
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SN74CBT3257
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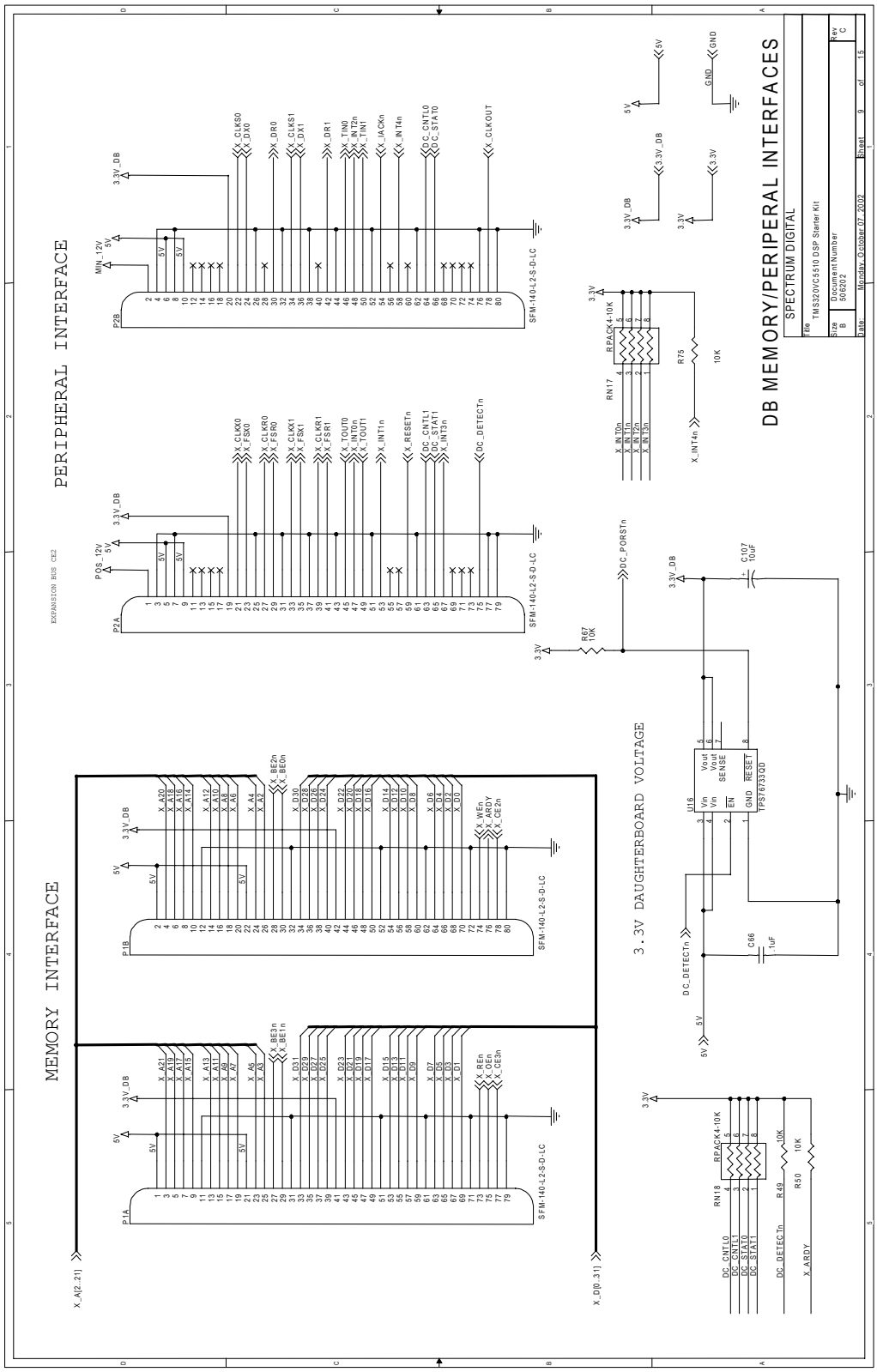
CPLD_ONBD_MCBSP2n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Size B Document Number 506202 Rev C
Date Monday, October 07, 2002 Sheet 9 of 15
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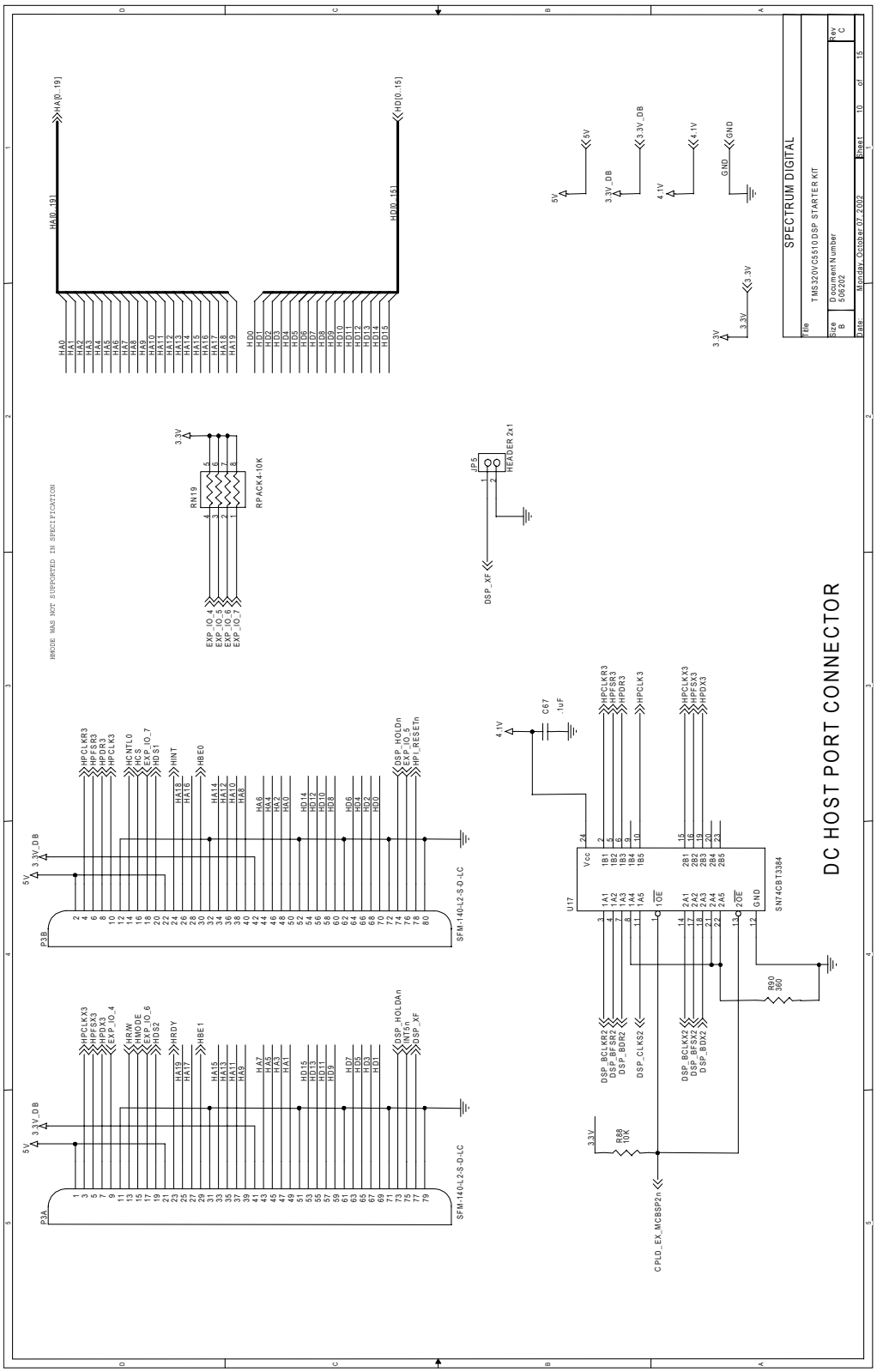
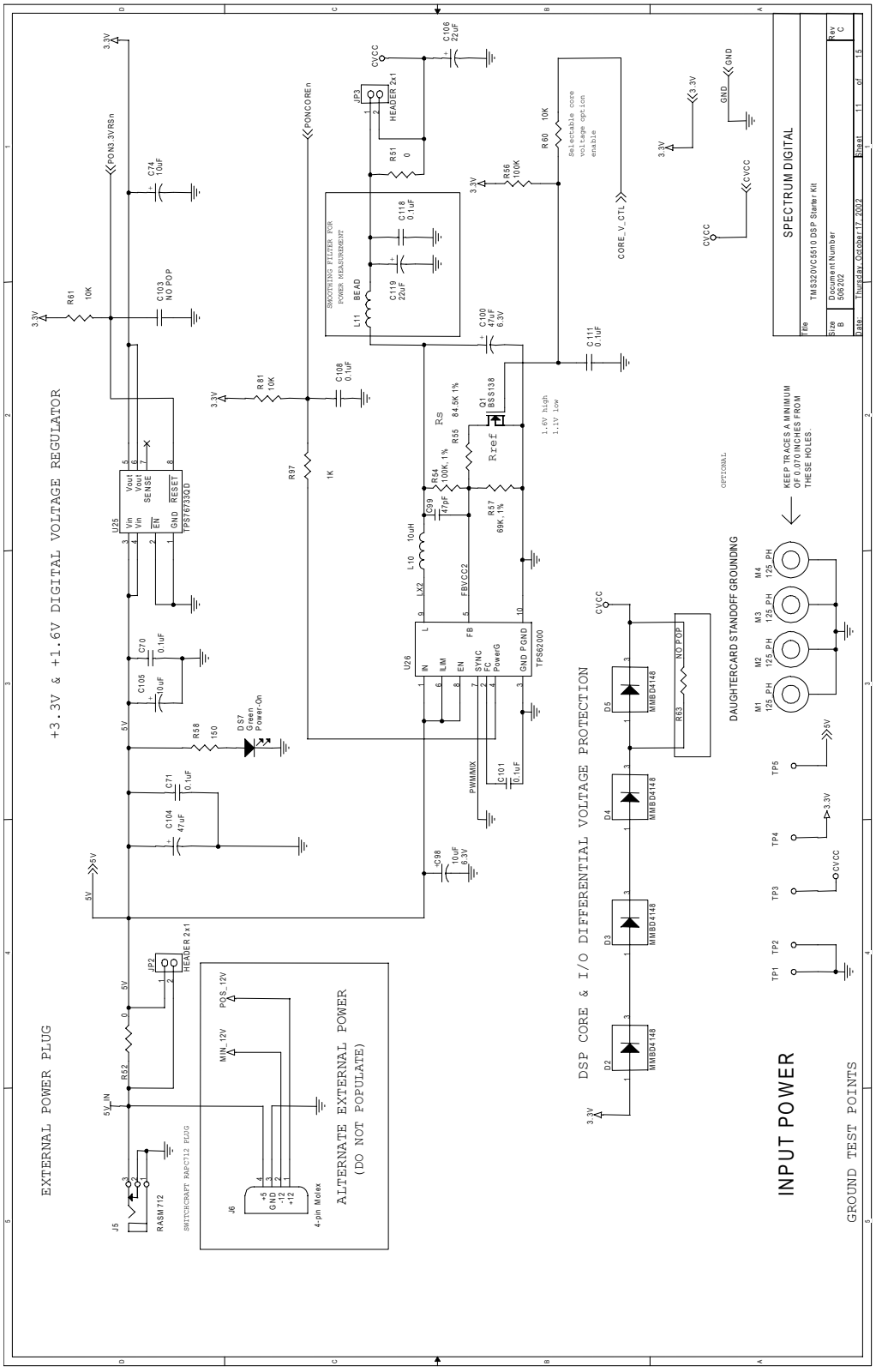
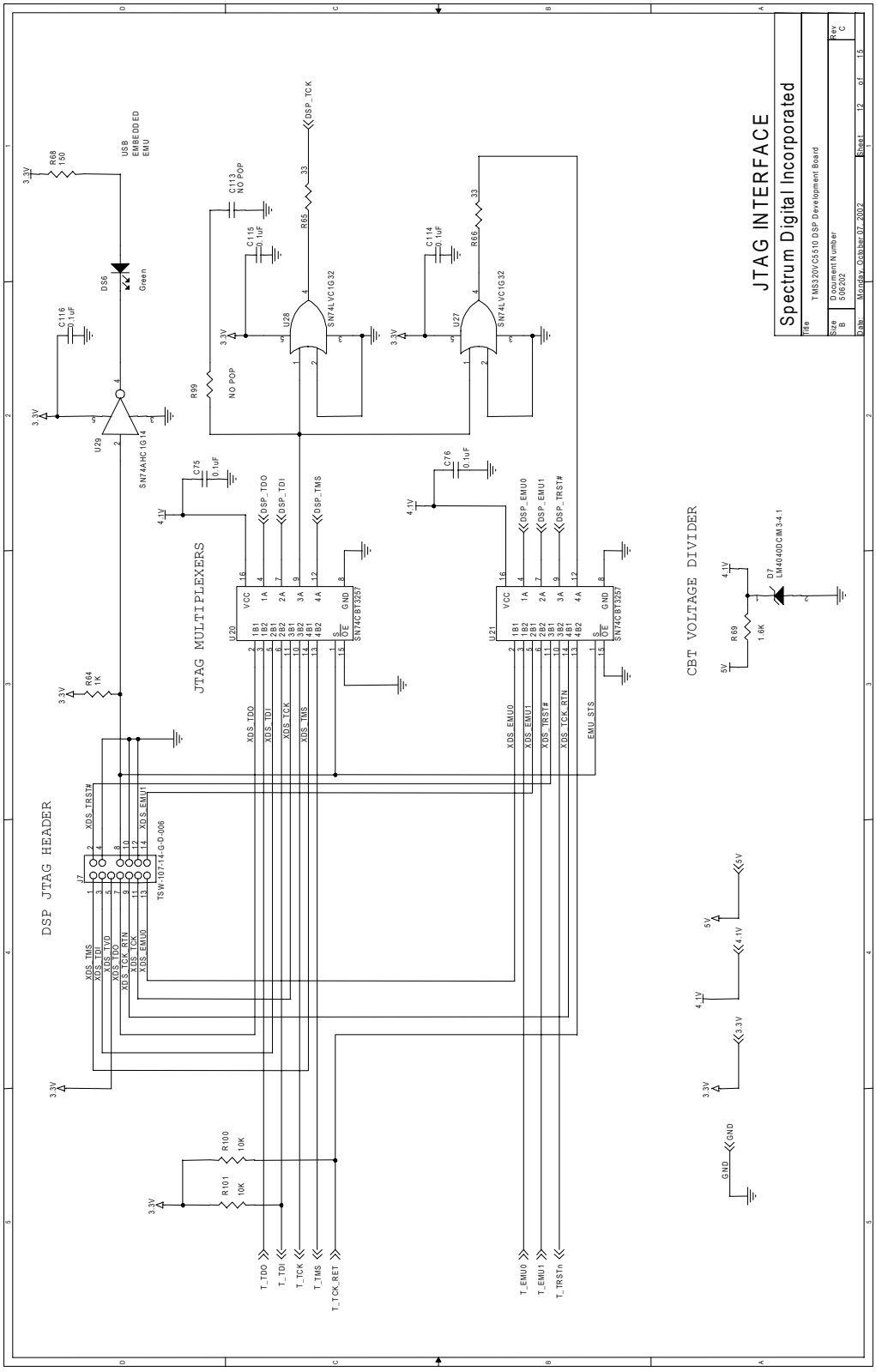
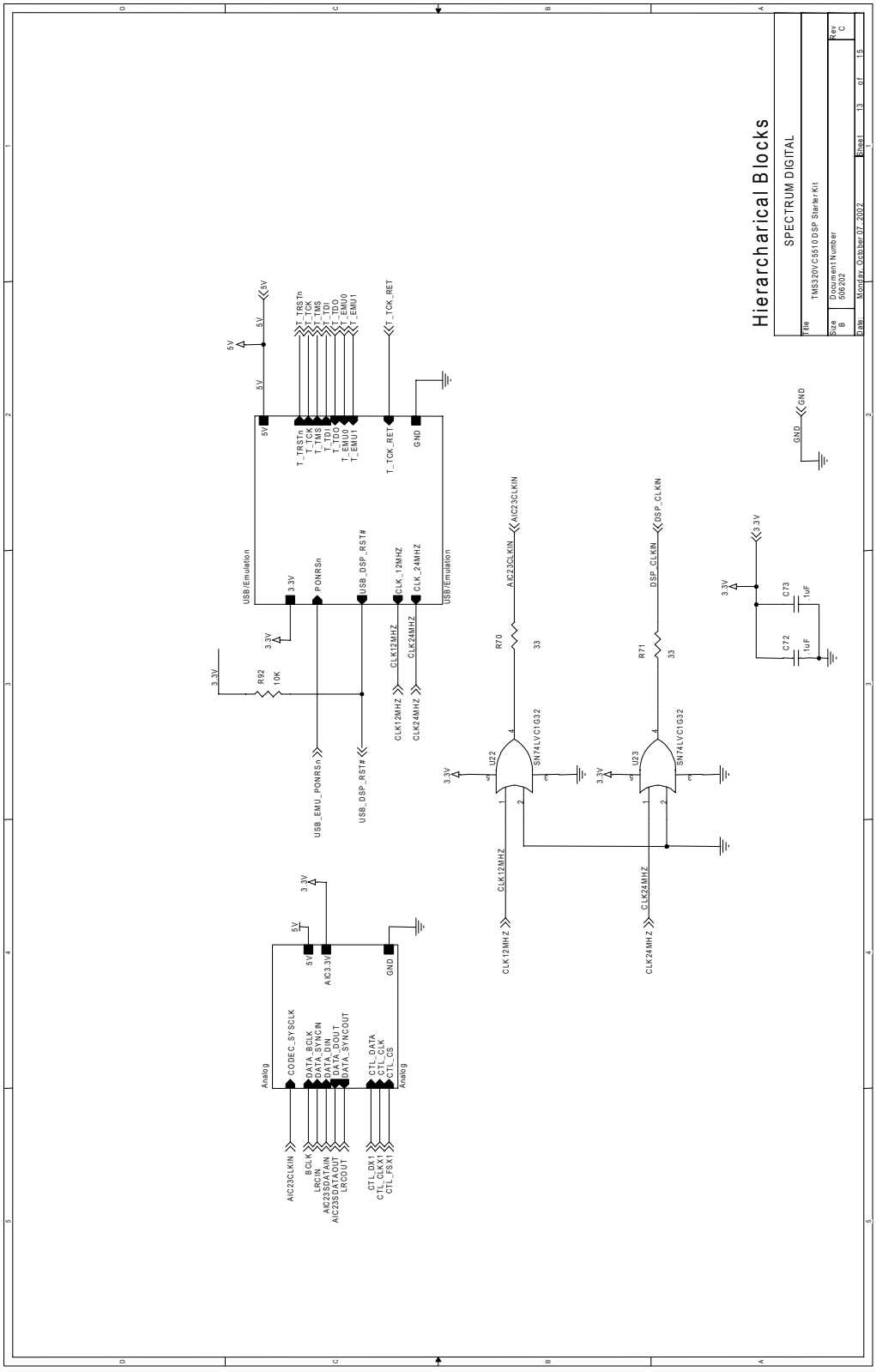
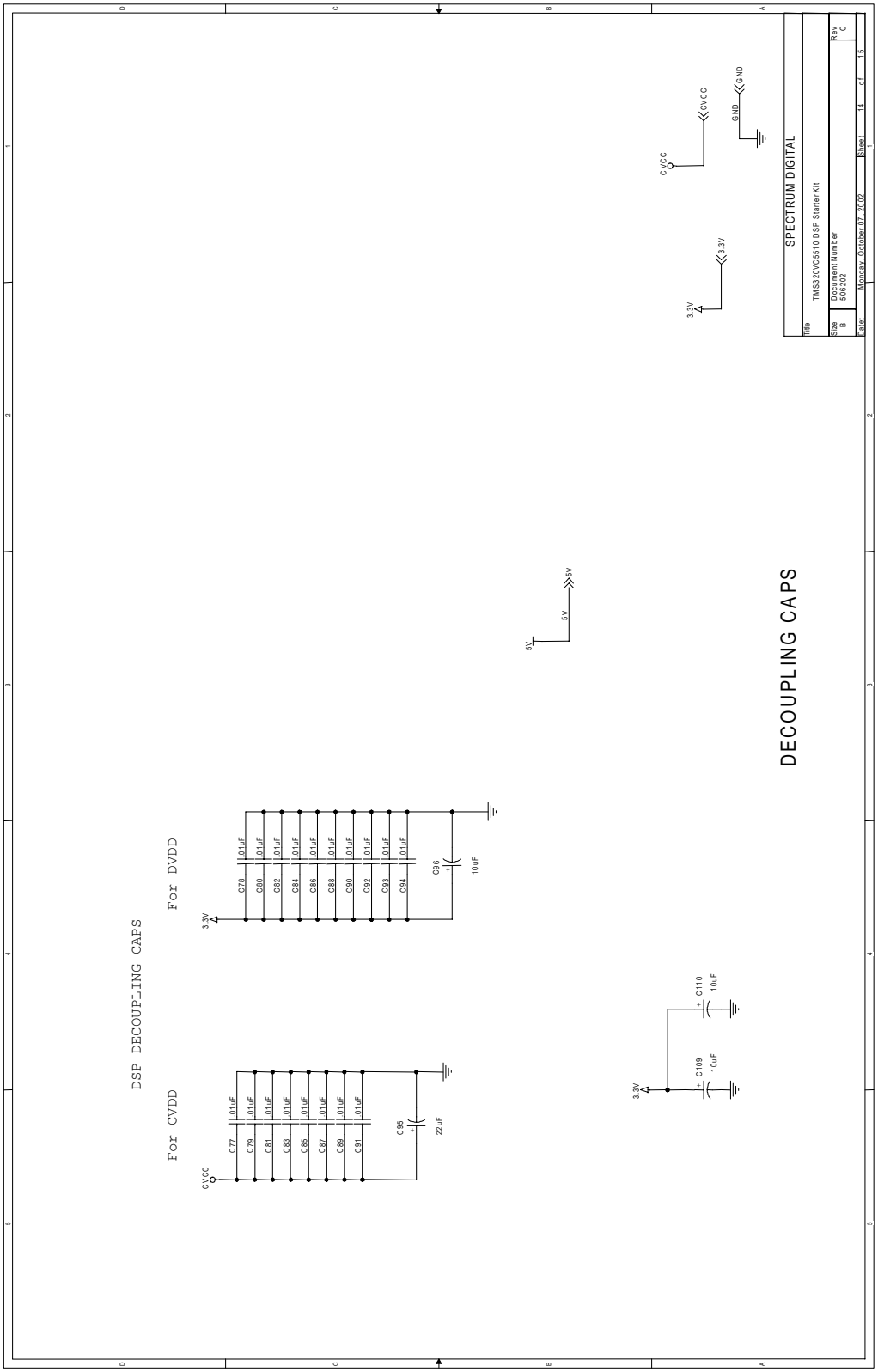
MEMORY INTERFACE
3.3V DAUGHTERBOARD VOLTAGE
EXPANSION BUS CE2
P2B
P2A
P1B
P1A
SFM-140-L2-S-D-LC
RPACK4-10K
RN17
RN18
R75
10K
R67
10K
R49
R50
C107
10uF
C66
.1uF
U16
TPS76733QD
X_A[2..21]
X_D[0..31]
DC_DETECTn
X_ARDY
DC_CNTL0
DC_CNTL1
DC_STAT0
DC_STAT1
X_INT4n
X_CLKOUT
3.3V_DB
5V
3.3V
GND

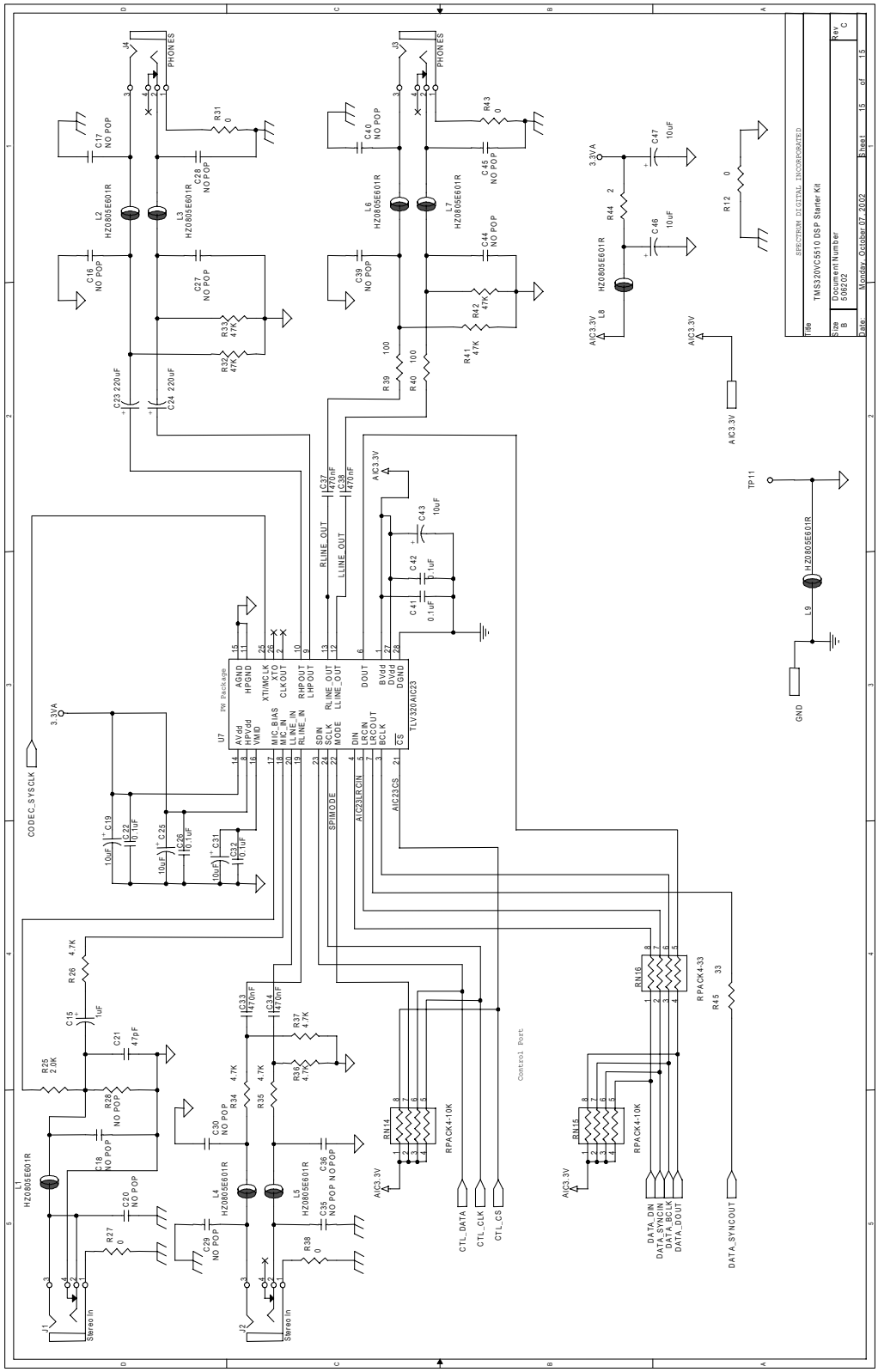

DC HOST PORT CONNECTOR
SPECTRUM DIGITAL
TMS320VC5510 DSP STARTER KIT
Monday, October 07, 2002
HMODE WAS NOT SUPPORTED IN SPECIFICATION
SFM-140-L2-S-D-LC
SN74CB73384
RPACK4-10K
HEADER 2x1
CPLD_EX_MCBSP2n
DSP_XF


+3.3V & +1.6V DIGITAL VOLTAGE REGULATOR
EXTERNAL POWER PLUG
ALTERNATE EXTERNAL POWER
(DO NOT POPULATE)
DSP CORE & I/O DIFFERENTIAL VOLTAGE PROTECTION
INPUT POWER
GROUND TEST POINTS
DAUGHTERCARD STANDOFF GROUNDING
KEEP TRACES A MINIMUM OF 0.070 INCHES FROM THESE HOLES.
SMOOTHING FILTER FOR POWER MEASUREMENT
Selectable core voltage option enable
1.6V high
1.1V low
OPTIONAL
SPECTRUM DIGITAL
TMS320VC5510 DSP Starter Kit
Document Number
506202
Thursday, October 17, 2002
U25 TPS76733QD
U26 TPS62000
Q1 BSS138
D57 Green Power-On
J5 RASM712
J6 4-pin Molex
JP2 HEADER 2x1
JP3 HEADER 2x1
D2 MMBD4148
D3 MMBD4148
D4 MMBD4148
D5 MMBD4148


JTAG INTERFACE
Spectrum Digital Incorporated
TMS320VC5510 DSP Development Board
Monday, October 07, 2002
JTAG MULTIPLEXERS
DSP JTAG HEADER
CBT VOLTAGE DIVIDER
USB EMBEDDED EMU
DS6
Green
SN74AHC1G14
SN74LVC1G32
SN74CBT3257
TSW-107-14-G-D-006
LM4040DCIM3-4.1
XDS_TDO
XDS_TDI
XDS_TCK
XDS_TMS
XDS_EMU0
XDS_EMU1
XDS_TRST#
XDS_TCK_RTN
EMU_STS
DSP_TDO
DSP_TDI
DSP_TMS
DSP_TCK
DSP_EMU0
DSP_EMU1
DSP_TRST#
T_TDO
T_TDI
T_TCK
T_TMS
T_TCK_RET
T_EMU0
T_EMU1
T_TRSTn
3.3V
4.1V
5V
GND


Hierarchical Blocks
SPECTRUM DIGITAL
TMS320VC5510 DSP Starter Kit
Document Number
506202
Monday, October 07, 2002
USB/Emulation
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TCK_RET
GND
PONRSn
USB_DSP_RST#
CLK_12MHZ
CLK_24MHZ
R92
10K
R70
33
R71
33
U22
U23
SN74LVC1G32
AIC23CLKIN
DSP_CLKIN
C73
.1uF
C72
.1uF
Analog
CODEC_SYSCLK
DATA_BCLK
DATA_SYNCIN
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
CTL_DATA
CTL_CLK
CTL_CS
AIC3.3V
BCLK
LRCIN
AIC23SDATAIN
AIC23SDATAOUT
LRCOUT
CTL_DX1
CTL_CLKX1
CTL_FSX1

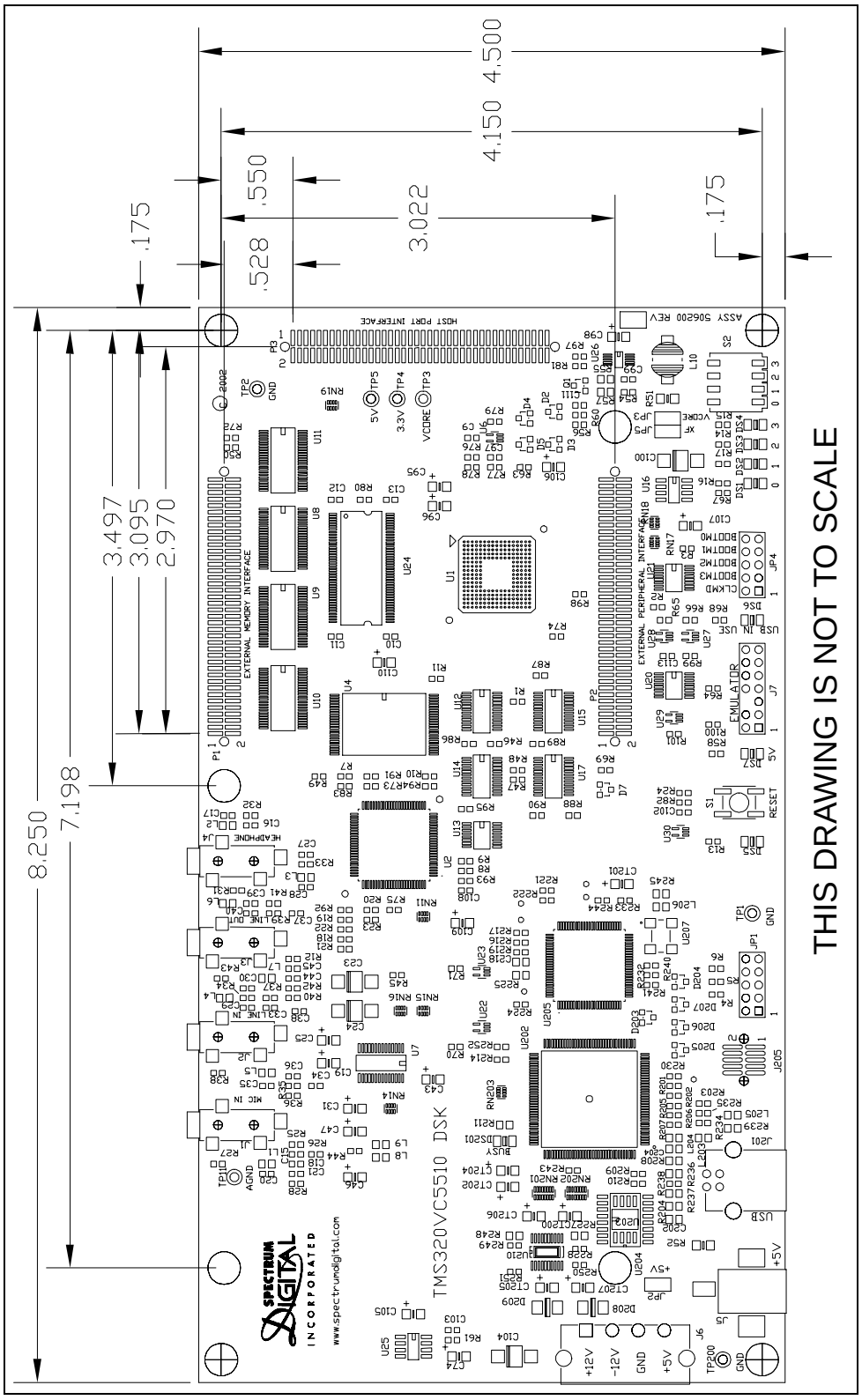

DECOUPLING CAPS
DSP DECOUPLING CAPS
For DVDD
For CVDD
SPECTRUM DIGITAL
TMS320VC5510 DSP Starter Kit
Document Number
506202
Monday, October 07, 2002
Rev C
Sheet 14 of 15
Size B
Date:
Title
CVCC
GND
3.3V
5V
C78 C80 C82 C84 C86 C88 C90 C92 C93 C94 0.1uF
C96 10uF
C77 C79 C81 C83 C85 C87 C89 C91 0.1uF
C95 22uF
C109 C110 10uF


PHONES
PHONES
U7
TLV320AIC23
PW Package
AGND
HPGND
XTI/MCLK
XTO
CLKOUT
RHPOUT
LHPOUT
RLINE_OUT
LLINE_OUT
DOUT
BVdd
DVdd
DGND
AVdd
HPVdd
VMID
MIC_BIAS
MIC_IN
LLINE_IN
RLINE_IN
SDIN
SCLK
MODE
DIN
LRCIN
LRCOUT
BCLK
CS
3.3VA
A/C3.3V
CODEC_SYSCLK
AIC23LRCIN
AIC23CS
SPIMODE
Control Port
CTL_DATA
CTL_CLK
CTL_CS
DATA_DIN
DATA_SYNCIN
DATA_BCLK
DATA_DOUT
DATA_SYNCOUT
Stereo In
Stereo In
GND
SPECTRUM DIGITAL INCORPORATED
TMS320VC5510 DSP Starter Kit
Document Number
506202
Monday, October 07, 2002
Rev C

# Appendix B

# Mechanical Information

This appendix contains the mechanical information about the TMS320VC5510 DSK produced by Spectrum Digital.


4.500
4.150
.550
.528
3.022
.175
.175
8.250
7.198
3.497
3.095
2.970
THIS DRAWING IS NOT TO SCALE
TMS320VC5510 DSK
SPECTRUM DIGITAL INCORPORATED
www.spectrumdigital.com
HOST PORT INTERFACE
EXTERNAL MEMORY INTERFACE
EXTERNAL PERIPHERAL INTERFACE
EMULATOR
RESET
HEADPHONE
MIC IN
LINE IN
LINE OUT
USB
+12V
-12V
GND
+5V

[redacted]

SPECTRUM DIGITAL INCORPORATED

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506205-0001 Rev. C