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FSA3341 — High-Speed 4:1 USB2.0 / MHL™ Switch

Features

- Low On Capacitance: 4.2 pF / 5 pF MHL / USB (Typical)
- Low Power Consumption: 30 µA Maximum
- Supports MHL Rev. 2.0
- Three USB2.0 Paths
- MHL Data Rate: 4.0 Gbps
- Packaged in 16-Lead UMLP (1.8 x 2.6 mm)
- Over-Voltage Tolerance on All USB Ports: Up to 5.25 V without External Components

Applications

- Cell Phones and Digital Cameras

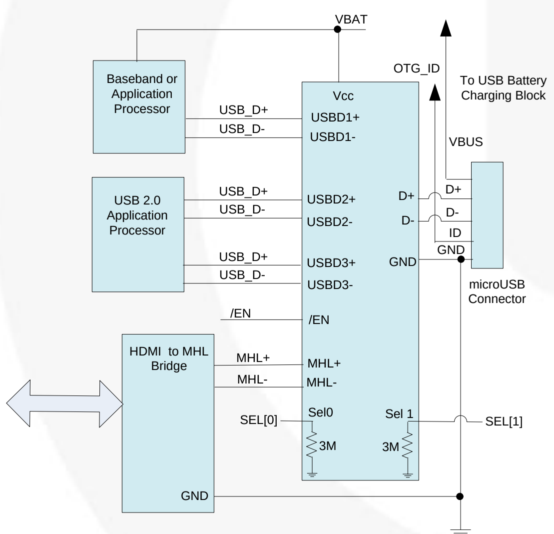

Figure 1. Typical Application

Description

The FSA3341 is a bi-directional, low-power, high-speed, 4:1, USB2.0 and MHL™ switch. Configured as a Double-Pole, Four-Throw (DP4T) switch; it is optimized for switching between high- or full-speed USB and Mobile High-Definition Link sources (MHL Rev. 2.0 specification). In addition, the USB2.0 paths can be used as UART paths.

The FSA3341 contains circuitry on the switch I/O pins that allows the device to withstand an over-voltage condition for applications where the V_{CC} supply is powered off (V_{CC} = 0 V). This switch is designed to minimize current consumption even when the control voltage applied to the control pins is lower than the supply voltage (V_{CC}). This is especially valuable in mobile applications, such as cell phones, allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, digital cameras, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3341UMX	LY	-40 to +85°C	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm

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Pin Configuration

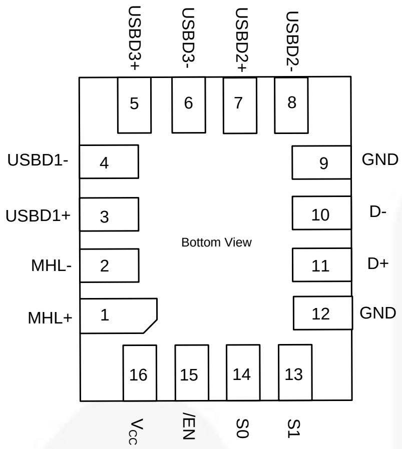


Figure 2. Pin Assignments

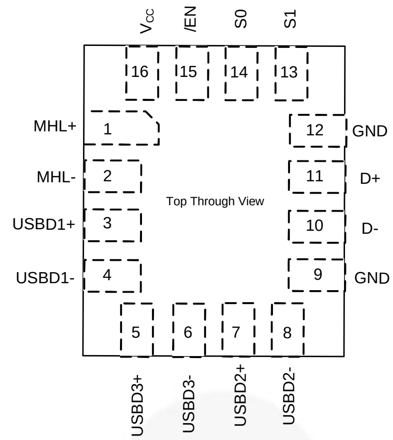


Figure 3. Top Through View

Pin Definitions

Pin#	Name	Description
1	MHL+	MHL Differential Data (Positive)
2	MHL-	MHL Differential Data (Negative)
3	USBD1+	USB Differential Data (Positive); also can be used as additional UART
4	USBD1-	USB Differential Data (Negative); also can be used as additional UART
5	USBD3+	USB Differential Data (Positive); also can be used as additional UART
6	USBD3-	USB Differential Data (Negative); also can be used as additional UART
7	USBD2+	USB Differential Data (Positive); can be used as a UART port *(see Figure 1)*
8	USBD2-	USB Differential Data (Negative); can be used as a UART port *(see Figure 1)*
9	GND	Ground
10	D-	USB Differential Data (Negative), Common Port
11	D+	USB Differential Data (Positive), Common Port
12	GND	Ground
13	S1	Data Switch Select *(see Table 1)*
14	S0	Data Switch Select *(see Table 1)*
15	/EN	Enable Pin - Active LOW
16	V_{CC}	Device Power from System (Typically V_{BAT})

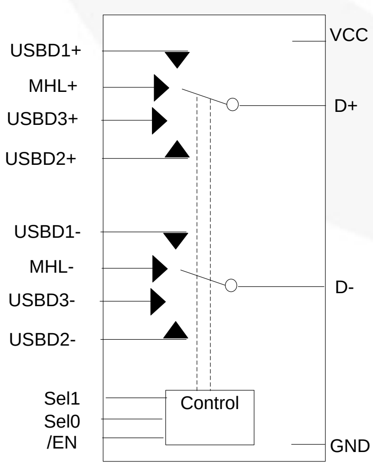


Figure 4. Analog Symbol

Table 1. Data Switch Select Truth Table

SEL1[1]	SEL0[1]	/EN[1]	Function
0	0	0	D+/D- connected to USBD1+/ USBD1- (or UART) path
0	1	0	D+/D- connected to USBD2+/USBD2- (or UART) path
1	0	0	D+/D- connected to MHL+/MHL- path
1	1	0	D+/D- connected to USBD3+/USBD3- (or UART) path
X	X	1	D+/D- high impedance

Note:

1. Control inputs should never be left floating or unconnected. To guarantee default switch closure to the USB position, the SEL[0:1] pins are tied to GND with internal weak pull-down resistors (3 MΩ) to minimize static current draw.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{CNTRL}	DC Input Voltage (/EN, SEL[1:0])(2)		-0.5	V_{CC}	V
V_{SW}(3)	DC Switch I/O Voltage(2)	USB, MHL	-0.5	V_{CC}	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	Switch DC Output Current (Continuous)	USB, MHL		60	mA
$I_{OUTPEAK}$	Switch DC Output Peak Current (Pulsed at 1 ms Duration, <10% Duty Cycle)	USB, MHL		150	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level: JEDEC J-STD-020A			1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		4	kV
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins(4)	Contact		8	
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins(4)	Air		15	
	Charged Device Model, JESD22-C101			2	

Notes:
2. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
3. V_{SW} refers to analog data switch paths (USB, MHL, and audio).
4. Testing performed in a system environment using TVS diodes.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	4.5	V
$t_{RAMP(VCC)}$	Power Supply Slew Rate	100	1000	µs/V
V_{CNTRL}	Control Input Voltage (/EN, SEL[1:0])(5)	0	4.5	V
$V_{SW(USB)}$	Switch I/O Voltage (USB Switch Path)	-0.5	3.6	V
Θ_{JA}	Thermal Resistance		273	C°/W
$V_{SW(MHL)}$	Switch I/O Voltage (MHL Switch Path)	1.65	3.45	V
T_A	Operating Temperature	-40	+85	°C

Note:
5. The control inputs must be held HIGH or LOW; they must not float.

DC Electrical Characteristics

All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=-40°C to +85°C			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.5			-1.2	V
V_{IH}	Control Input Voltage HIGH	SEL[1:0]	2.5	1.3			V
			3.6	1.4			V
			4.5	1.5			V
V_{IL}	Control Input Voltage LOW	SEL[1:0]	2.5			0.4	V
			3.6			0.4	V
			4.5			0.4	V
I_{IN}	Control Input Leakage SEL[1:0]	V_{SW} (MHL & USB)=0 to 3.6 V, V_{CNTRL}=0 to V_{CC}	4.5	-2.5		2.5	µA
$I_{OZ(MHL)}$	Off-State Leakage for Open MHL Data Paths	V_{SW}=1.65 ≤ MHL ≤ 3.45 V, /EN=V_{CC}, Figure 6	4.5	-0.5		0.5	µA
$I_{OZ(USB)}$	Off-State Leakage for Open USB Data Paths	V_{SW}=0 ≤ USB≤ 3.6 V, /EN=V_{CC}, Figure 6	4.5	-0.5		0.5	µA
$I_{CL(MHL)}$	On-State Leakage for Closed MHL Data Paths(6)	V_{SW}=1.65 ≤ MHL ≤ 3.45 V, /EN=GND, SEL0=GND, SEL1=V_{CC}	4.5	-0.5		0.5	µA
$I_{CL(USB)}$	On-State Leakage for Closed USB Data Paths(6)	V_{SW}=0 ≤ USB ≤ 3.6 V, /EN=GND, SEL[1:0]=GND and SEL1=GND, SEL0=V_{CC}	4.5	-0.5		0.5	µA
I_{OFF}	Power-Off Leakage Current (USB & MHL Paths)	V_{SW}=0 V or 3.6 V, Figure 6	0	-0.5		0.5	µA
$R_{ON(USB)}$	HS Switch On Resistance (USBDn to Dn Path)	V_{SW}=0.4 V, I_{ON}=-8 mA, SEL[1:0]=GND, and SEL1=GND, SEL0=V_{CC} Figure 5	2.5 to 4.5		8		Ω
$R_{ON(MHL)}$	HS Switch On Resistance (MHL to D Path)	V_{SW}=V_{CC}-1050 mV, SEL0=GND, SEL1=V_{CC}, I_{ON}=- 8 mA, Figure 5	2.5 to 4.5		5		Ω
$\Delta R_{ON(MHL)}$	Difference in R_{ON} Between MHL Positive-Negative	V_{SW}=V_{CC}-1050 mV, SEL0=GND, SEL1=V_{CC}, I_{ON}=-8 mA, Figure 5,	2.5 to 4.5		0.03		Ω
$\Delta R_{ON(USB)}$	Difference in R_{ON} Between USB Positive-Negative	V_{SW}=0.4V, I_{ON}=-8 mA, SEL[1:0]=GND and SEL1=GND, SEL0=V_{CC}, Figure 5	2.5 to 4.5		0.18		Ω
$R_{ONF(MHL)}$	Flatness for R_{ON} MHL Path	V_{SW}=1.65 V to 3.45 V, SEL0=GND, SEL1=V_{CC}, I_{ON}=-8 mA, Figure 5	2.5 to 4.5		1		Ω
$R_{ONFD(USB)}$	Flatness for R_{ON} USB Path	V_{SW}=0 V to 3.6 V, SEL[1:0]=GND and SEL1=GND, SEL0=V_{CC}, I_{ON}=-8 mA, Figure 5	2.5 to 4.5		2.1		Ω
R_{PD}	Internal Pull -Down Resistors on SEL0 & SEL1		2.5 to 4.5		3		MΩ
I_{CC}	Quiescent Current	V_{CNTRL}=0 or 4.5 V, I_{OUT}=0	4.5			30	µA
I_{CCZ}	Quiescent Current-High Impedance	$V_{/EN}$=4.5 V, I_{OUT}=0	4.5			1	µA
I_{CCT}	Delta Increase in Quiescent Current per Control Pin	V_{CNTRL}=1.65 V, I_{OUT}=0	4.5			10	µA
		V_{CNTRL}=2.5 V, I_{OUT}=0	4.5			5	

Note:
6. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3 V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=-40°C to +85°C			Unit
				Min.	Typ.	Max.	
t_{ONUSB}	USB Turn-On Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	700	ns
t_{OFFUSB}	USB Turn-Off Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t_{ONMHL}	MHL Turn-On Time, SEL[1:0] to Output	R_L=50 Ω to 3.3 V, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t_{OFFMHL}	MHL Turn-Off Time, SEL[1:0] to Output	R_L=50 Ω to 3.3 V, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t_{ENABLE}	Enable Turn-On Time, /EN to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		80		µs
$t_{DISABLE}$	Disable Turn-Off Time, /EN to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, Figure 7, Figure 8	2.5 to 4.5		35		ns
t_{PD}	Propagation Delay(7)	C_L=5 pF, R_L=50 Ω, Figure 7, Figure 9	2.5 to 4.5		0.25		ns
t_{BBM}	Break-Before-Make(7)	R_L=50 Ω, C_L=50 pF, V_{MHL}=3.3 V, V_{USB}=0.8 V, Figure 11	2.5 to 4.5	50	120	600	ns
$O_{IRR(MHL)}$	Off Isolation(7)	V_S=1 $V_{pk\text{-}pk}$, R_L=50 Ω, f=24 MHz, Figure 13	2.5 to 4.5		-36		dB
$O_{IRR(USB)}$		V_S=400 $mV_{pk\text{-}pk}$, R_L=50 Ω, f=240 MHz, Figure 13	2.5 to 4.5		-38		dB
$O_{IRR(UART)}$		V_S=40 $mV_{pk\text{-}pk}$, R_L=50 Ω, f=10 MHz, Figure 13	2.5 to 4.5		-40		dB
$Xtalk_{MHL}$	Non-Adjacent Channel Crosstalk(7)	V_S=1 $V_{pk\text{-}pk}$, R_L=50 Ω, f=240 MHz, Figure 14	2.5 to 4.5		-44		dB
$Xtalk_{USB}$		V_S=400 $mV_{pk\text{-}pk}$, R_L=50 Ω, f=240 MHz, Figure 14	2.5 to 4.5		-36		dB
$Xtalk_{UART}$		V_S=400 $mV_{pk\text{-}pk}$, R_L=50 Ω, f=10 MHz, Figure 14	2.5 to 4.5		-36		dB
THD	Total Harmonic Distortion - LINOUT(7)	R_T=600 Ω, V_{SW}=2 $V_{pk\text{-}pk}$, f=20 Hz to 20 kHz, V_{BIAS}=0 V	2.5 to 4.5		0.01		%
BW	S_{DD21} Differential -3db Bandwidth(7)	V_{IN}=1 $V_{pk\text{-}pk}$, Common Mode Voltage=V_{CC} – 1.1 V, MHL Path, R_L=50 Ω, C_L=0 pF, Figure 12	2.5 to 4.5		2.0		GHz
		V_{IN}=400 $mV_{pk\text{-}pk}$, Common Mode Voltage=0.2 V, USB Path, R_L=50 Ω, C_L=0 pF, Figure 12			650(8)		MHz

Note:

7. Guaranteed by characterization.
8. 650 MHz USB Bandwidth, passed USB2.0-Compliant testing.

USB High-Speed AC Electrical Characteristics

Typical values are at T_A=25°C and V_{CC}=3.0 to 3.6 V.

Symbol	Parameter	Condition	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(9)	C_L=5 pF, R_L=50 Ω, Figure 10	3	ps
t_J	Total Jitter(9)	R_L=50 Ω, C_L=5 pF, t_R=t_F=500 ps (10-90%) at 480 Mbps, PN7	20	ps

Note:
9. Guaranteed by characterization.

MHL™ AC Electrical Characteristics

Typical values are at T_A=25°C and V_{CC}=3.0 to 3.6 V.

Symbol	Parameter	Condition	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(10)	R_{PU}=50 Ω to V_{CC}, C_L=0 pF	2	ps
t_J	Total Jitter(10)	f=2.25 Gbps, PN7, R_{PU}=50 Ω to V_{CC}, C_L=0 pF	15	ps

Note:
10. Guaranteed by characterization.

Capacitance

Typical values are at T_A = 25ºC.

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Control Pin Input Capacitance(11)	V_{CC}=0V, f=1 MHz	2.5	pF
$C_{ON(USB)}$	USB Path On Capacitance(11)	V_{CC}=3.3 V, f=240 MHz, Figure 16	5.0	
$C_{OFF(USB)}$	USB Path Off Capacitance(11)	V_{CC}=3.3 V, f=240 MHz, Figure 15	2.5	
$C_{ON(MHL)}$	MHL Path On Capacitance(11)	V_{CC}=3.3 V, f=240 MHz, Figure 16	4.2	
$C_{OFF(MHL)}$	MHL Path Off Capacitance(11)	V_{CC}=3.3 V, f=240 MHz, Figure 15	2.5	

Note:
11. Guaranteed by characterization.

Test Diagrams

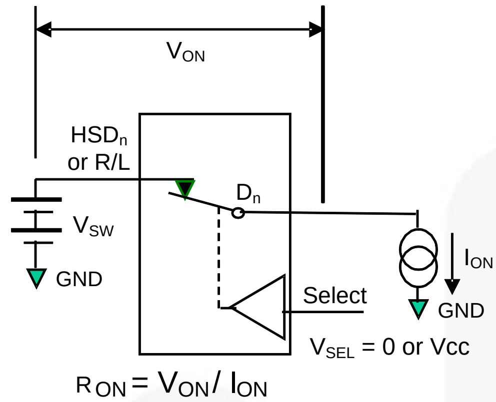


Figure 5. On Resistance

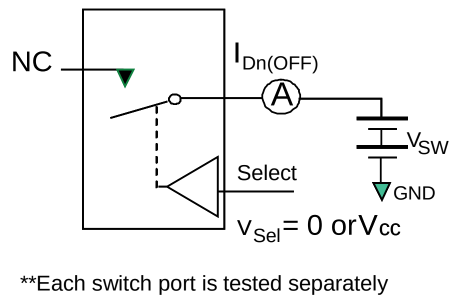


Figure 6. Off Leakage

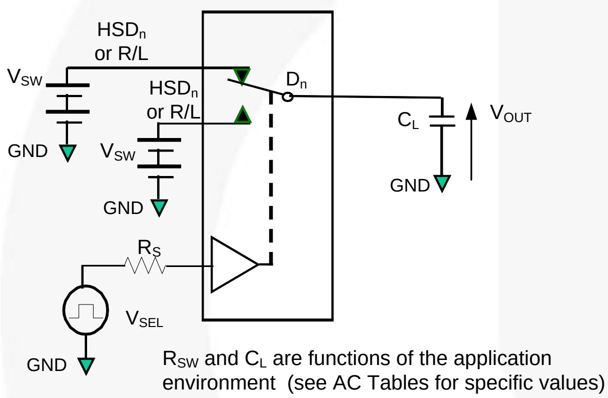


Figure 7. AC Test Circuit Load

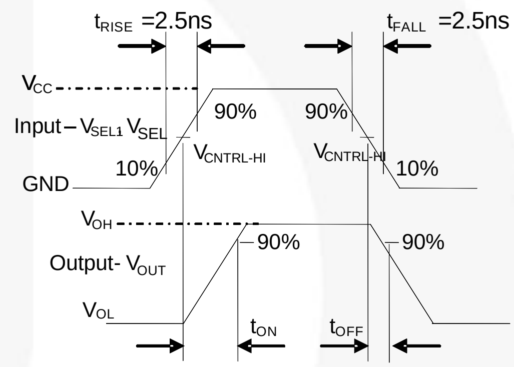


Figure 8. Turn-On / Turn-Off Waveforms

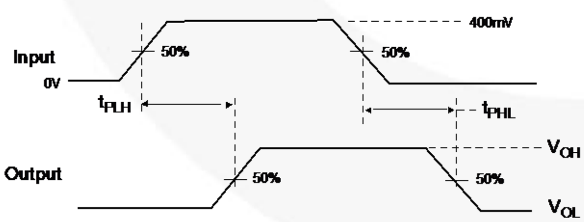


Figure 9. Propagation Delay ($t_R t_F$ – 500 ps)

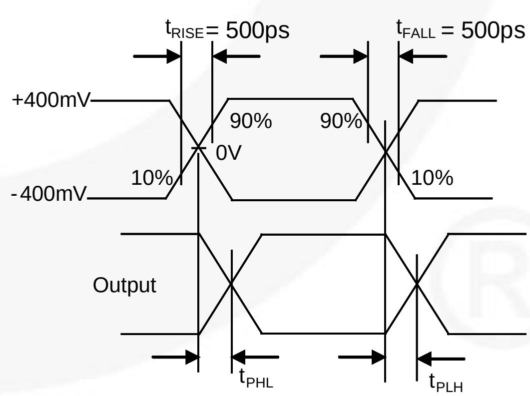
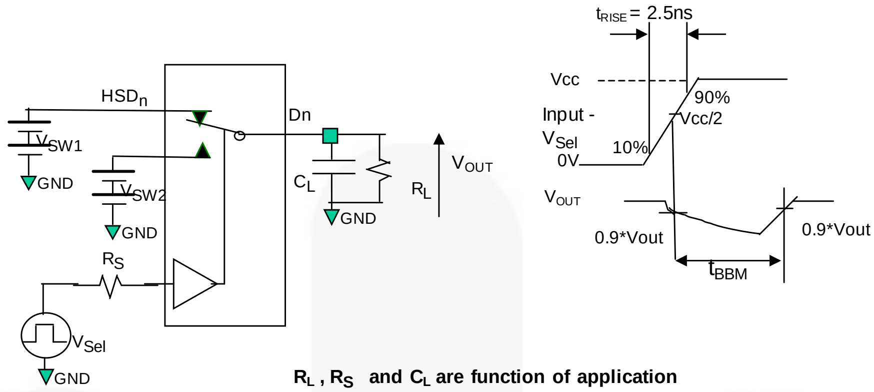


Figure 10. Intra-Pair Skew Test $t_{SK(P)}$

Note:

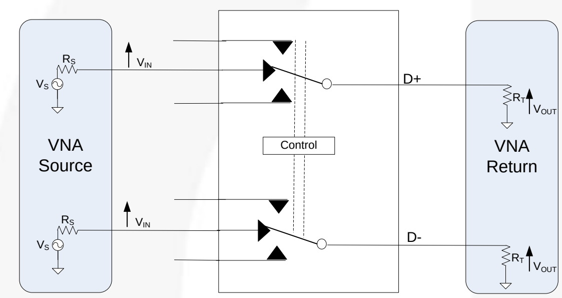
12. HSD_n refers to the high-speed data USB or MHL paths.

Test Diagrams (Continued)



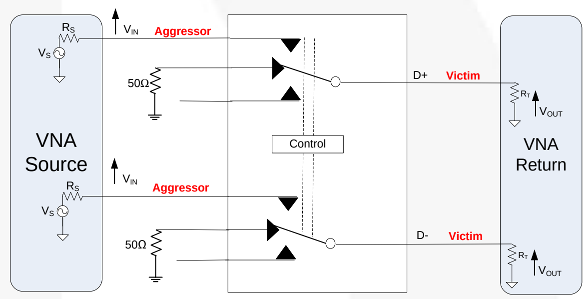
R_L , R_S and C_L are function of application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 11. Break-Before-Make Interval Timing



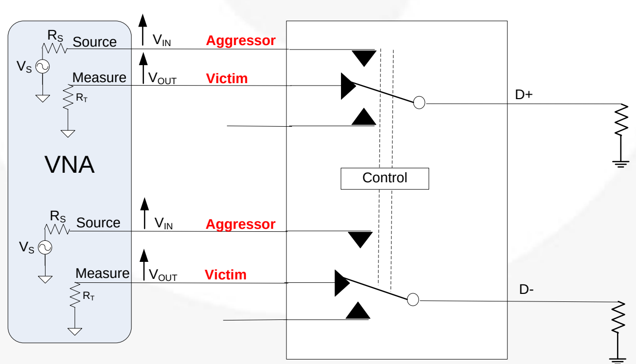
V_S, R_S and R_T are functions of the application environment (see AC/DC Tables for values).

Figure 12. Insertion Loss (SDD21)



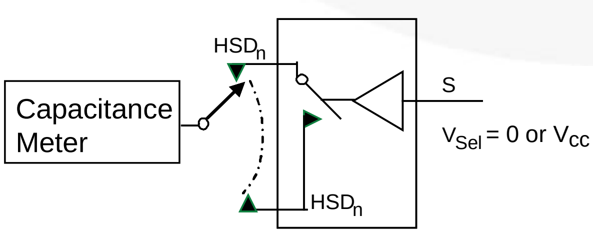
V_S, R_S and R_T are functions of the application environment (see AC/DC Tables for values).
Off Isolation = 20 Log (V_{OUT} - V_{IN})

Figure 13. Channel Off Isolation (SDD21)



V_S, R_S, and R_T are functions of the application environment (*see AC-DC Tables for values*).
Off Isolation = 20 Log (V_{OUT} - V_{IN})

Figure 14. Non-Adjacent Channel-to-Channel Crosstalk (SDD21)



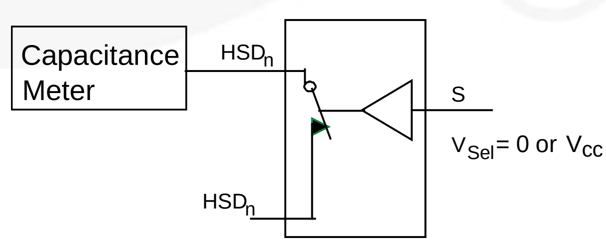


Figure 15. Channel Off Capacitance

Figure 16. Channel On Capacitance

Functional Description

Insertion Loss

One of the key advantages of using the FSA3341 in mobile digital-video applications is the small amount of insertion loss experienced by the received signal as it passes through the switch. This results in minimal degradation to the received eye. One of the ways to measure the quality of the high-data-rate channels is using balanced ports and four-port differential S-parameter analysis, particularly SDD21.

Bandwidth is measured using the S-parameter SDD21 methodology.

Typical Applications

Figure 19 shows the FSA3341 utilizing the V_{BAT} connection. The 3 MΩ resistors are used to ensure, for manufacturing test via the micro-USB connector, that the FSA3341 configures for connectivity to the baseband or application processor.

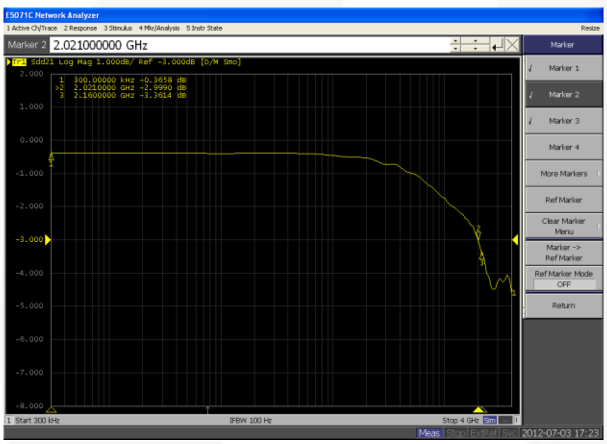


Figure 17. MHL Path SDD21 Insertion Loss Curve

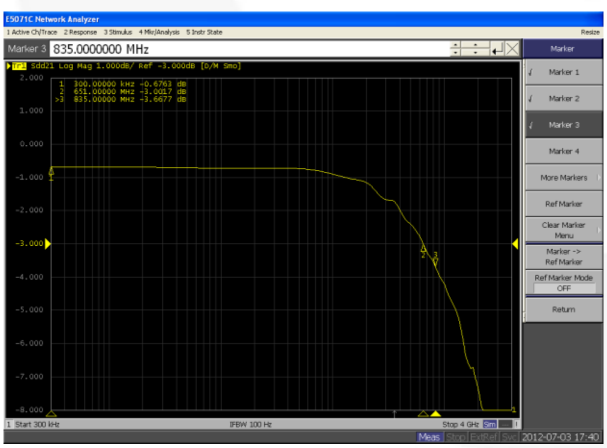


Figure 18. USB Path SDD21 Insertion Loss Curve

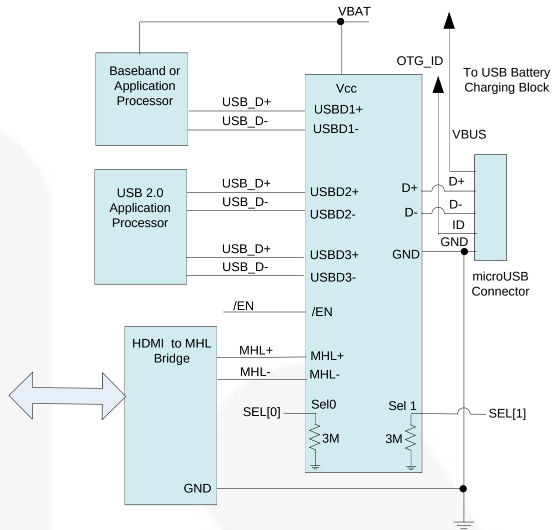
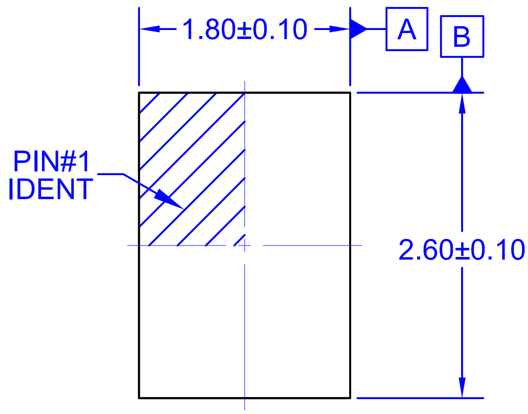
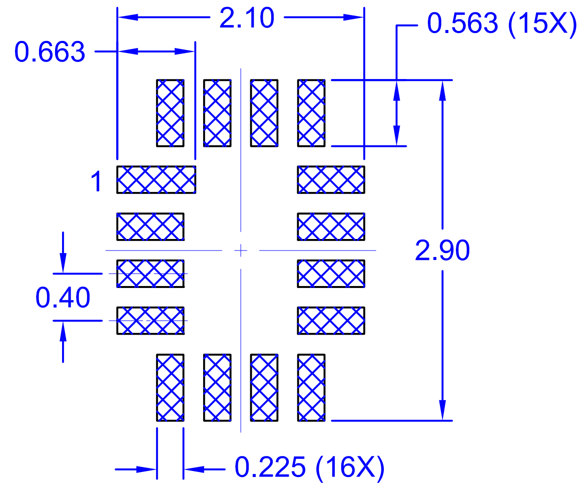


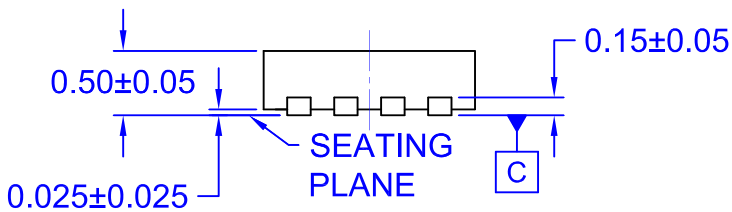
Figure 19. Typical Application



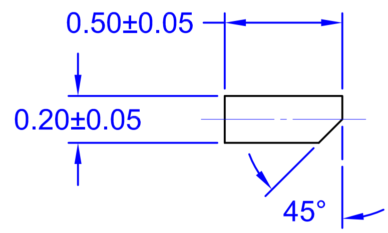
TOP VIEW



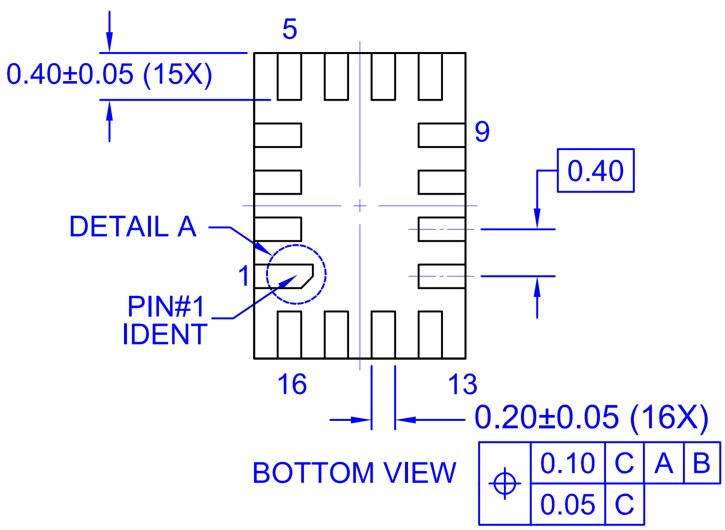
RECOMMENDED
LAND PATTERN



SIDE VIEW

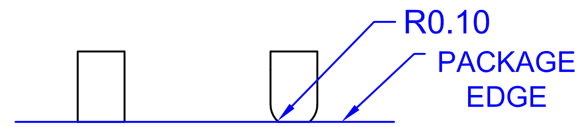


DETAIL A
SCALE 2:1



BOTTOM VIEW

LEAD SHAPE AT PACKAGE EDGE



LEAD
OPTION 1
SCALE 2:1

LEAD
OPTION 2
SCALE 2:1

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

D DRAWING FILENAME: MKT-UMLP16ArevG.

E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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