Si468x Schematics and Layout Guide

1. Introduction

This document provides the following:

- General Si468x design guidelines, which include schematics, layout, and BOM
- Si468x AM/AMHD-FM/FMHD-DAB/DAB+ antenna/matching network design guidelines

2. Si468x QFN Schematic and Layout

2.1. Schematic design and component selection

This section shows the minimal schematic and layout options reserved for optimal performance of the Si468x in the QFN package. Population options are provided to mitigate on-chip VCO radiated emissions, to use analog audio output, and to operate the Si468x with crystal.

2.1.1. Schematic Design

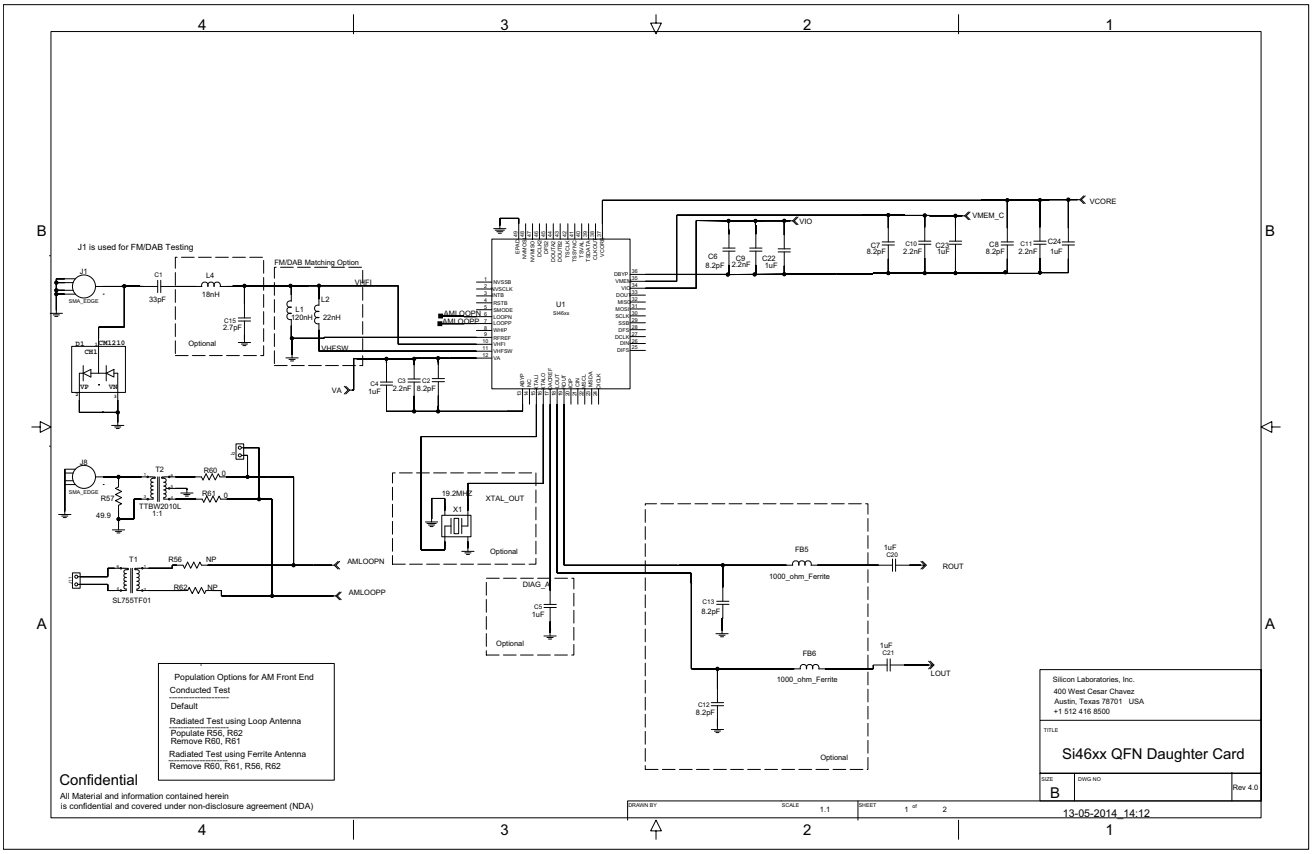


Figure 1. Si468x QFN Schematic Design

3. EMI Mitigation

Due to a high frequency (2880–3840 MHz) on-chip VCO, there is some conductive and magnetic coupling from the VCO to the adjacent traces. The VCO fundamental spur level can be reduced by adding external filtering and using the proper layout.

3.1. External filtering

- Add filter network comprising of L4 and C15 on the RF input trace (VHFI) for filtering the VCO spur (2880–3840 MHz). The capacitance C15 provides a low impedance path to ground, and inductor L4 provides high impedance to the VCO spur. The inductor L4 also helps in protecting the chip from an external ESD event by providing high impedance path to the ESD event. The two component network attenuates the VCO spur from reaching external antenna port and radiating out. The values of these components are selected to achieve the balance between the sensitivity and the emission levels.
- Add low pass network C13 & FB5 and C12 & FB6 on the audio lines Right and Left respectively for attenuating the VCO coupling
- Add high Self Resonant Frequency (>3 GHz) capacitors C2, C6, C7 and C8 on the supply lines to decouple the VCO leakage currents.

3.2. Front-End Matching

The components (C1, L1, L2, and L4) are used for maximizing the voltage gain on the VHFI pin.

For the FM and DAB band, the matching components C1, L1, L2, and L4 will require optimization to maximize the voltage gain on the VHFI pin. The inductor L2 can be engaged or disengaged using a VHFSW switch. Refer to property “0x1712” of AN649 for information on how to handle the VHFSW switch. The voltage gain is maximized by forming a high Q parallel LC resonant tank circuit. The inductor of the tank circuit is the parallel combination of L1 and L2. And the tank capacitance includes the antenna capacitance, capacitance of the external front end network, PCB parasitic, internal chip parasitic and internal variable capacitance provided by on-chip varactor tuning.

With a given antenna source impedance and the parasitics (pcb and chip internal), the resonant peak of the LC tank circuit across the FM and DAB band can be maximized by finding the right combination of C1, L1, L2, and L4, and the internal varactor capacitance. Refer to Appendix A for additional details on using internal varactor tuning. Note that the procedure outlined in Appendix A for internal varactor tuning is considering the signal generator source impedance (50 Ω) but the same procedure can be used with different antenna source impedance. Refer to Appendix B on how to select component values for optimizing the front end.

Table 1. Application Schematic BOM

Ref Designator	Description	Value	Manufacture Part #
C1	CAP,SM,0402	33 pF	C0402C0G500-330JNP
L4	IND,SM,0402	18 nH	LQG15HS18NJ02D
C15	CAP,SM,0402	2.7 pF	GJM1555C1H2R7BB01D
L1	IND,SM,0402	120 nH	LQW15ANR12J00D
L2	IND,SM,0402	22 nH	LQW15AN22NH00D
C2,C6,C7,C8,C12 and C13	CAP,SM,0402	8.2 pF	GRM1555C1H8R2DA01D
FB5 and FB6	Ferrite, 0402	1000 ohm	BLM15HG102SN1D
C3,C9,C10 and C11	CAP,SM,0402	2.2 nF	C0402X7R500-222KNP
C1, C20, C21, C22, C23, and C24	CAP,SM,0402	1 µF	C1005X5R1C105K050BC
X1	Crystal	19.2	Abracon, ABM8-19.200MHz-10-1-U_T, 19.2 MHz
T2	Transformer for conducted measurement using signal generator	1:1	TTBW2010
T1	Transformer for radiated measurements with loop antenna	1:6	SL755TF01
R56 and R62	RES, SM, 0402	0 Ω	CR0402-16W-000T

3.2.1. Component Selection and Replacement

The front end network components shall be placed as close as possible to the chip and as far away from noise sources such as clocks and digital circuits. L1 shall be routed to ground plane with a short trace and a via connection.

The recommendations regarding C1, C2, C3, C5, C6, C7, C8, C9 and C10 are made to reduce the size of the current loop created by the bypass cap and routing, minimize impedance and return all currents to the ground.

C3 and C4 (2.2 nF and 1 uF) are **required** bypass capacitors for VA supply pin 12. Place C2, C3 and C4 as close as possible to VA. C3 and C4 are chosen to mitigate noise in medium to VHF frequency range. Place a via connecting C2, C3, C4 and VA pins to the power rail such that the caps are closer to the Si468x VA pin than the via. Route C2, C3 and C4 only to the ABYP pin directly with a short (6-mil width) low inductance trace.

C9 and C22 (2.2 nF and 1 uF) are **required** bypass capacitors for VIO supply pin 34. C9 and C22 are chosen to mitigate noise in medium to VHF frequency range. Place C6, C9, and C22 as close as possible to VIO pin 34 and DBYP pin 36. Place a via connecting C6, C9, and C22 and VIO supply to the power rail such that the caps are closer to the Si468x VIO pin than the via. Route C6, C9, and C22 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C10 and C23 (2.2nF and 1 uF) are **required** bypass capacitors for VMEM supply pin 35. C10 and C23 are chosen to mitigate noise in medium to VHF frequency range. Place C7, C10, and C23 as close as possible to VMEM pin 35 and DBYP pin 36. Place a via connecting C7, C10, and C23 and VMEM supply pin to the power rail such that the caps are closer to the Si468x VMEM pin than the via. Route C7, C10, and C23 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C11 and C24 (2.2nF and 1 uF) are **required** bypass capacitors for VCORE supply pin 37. C11 and C24 are chosen to mitigate noise in medium to VHF frequency range. Place C8, C11 and C24 as close as possible to VCORE pin 37 and DBYP pin 36. Place a via connecting C8, C11 and C24 and VCORE pin 37 to the power rail such that the caps are closer to the Si468x VCORE pin than the via. Route C8, C11 and C24 only to DBYP directly with a short (6-mil width) low inductance trace.

C5 (1uF) is an **optional** bypass capacitor for DACREF pin 17 if customer uses analog audio output. Place C4 as close as possible to DACREF pin. Customers do not need to populate this capacitor if they are using digital audio output only.

C20 and C21 (1uF) are **optional** ac coupling capacitors for analog audio outputs. The value should be selected to work well with the customer's choice of audio amp.

X1 is an **optional** crystal required only when using the internal oscillator feature. Place the crystal X1 as close to XTALI (pin 15) and XTALO (pin 16) as possible to minimize current loops.

3.3. Layout Guide

The following placement/layout guidelines are suggested for 4-layer PCB:

- PCB layer assignment:
- Layer 1 top side placement and routing for RF and analog traces
- Layer 2 ground plane
- Layer 3 routing for high frequency digital traces and ground plane
- Layer 4 bottom side placement and routing for low frequency digital traces
- Minimum 6-mil trace
- Minimum 6-mil trace spacing
- 6-mil drill 9-mil plating for normal vias
- Minimum 10-mil component spacing
- Power routed by trace
- 0402 component size or larger

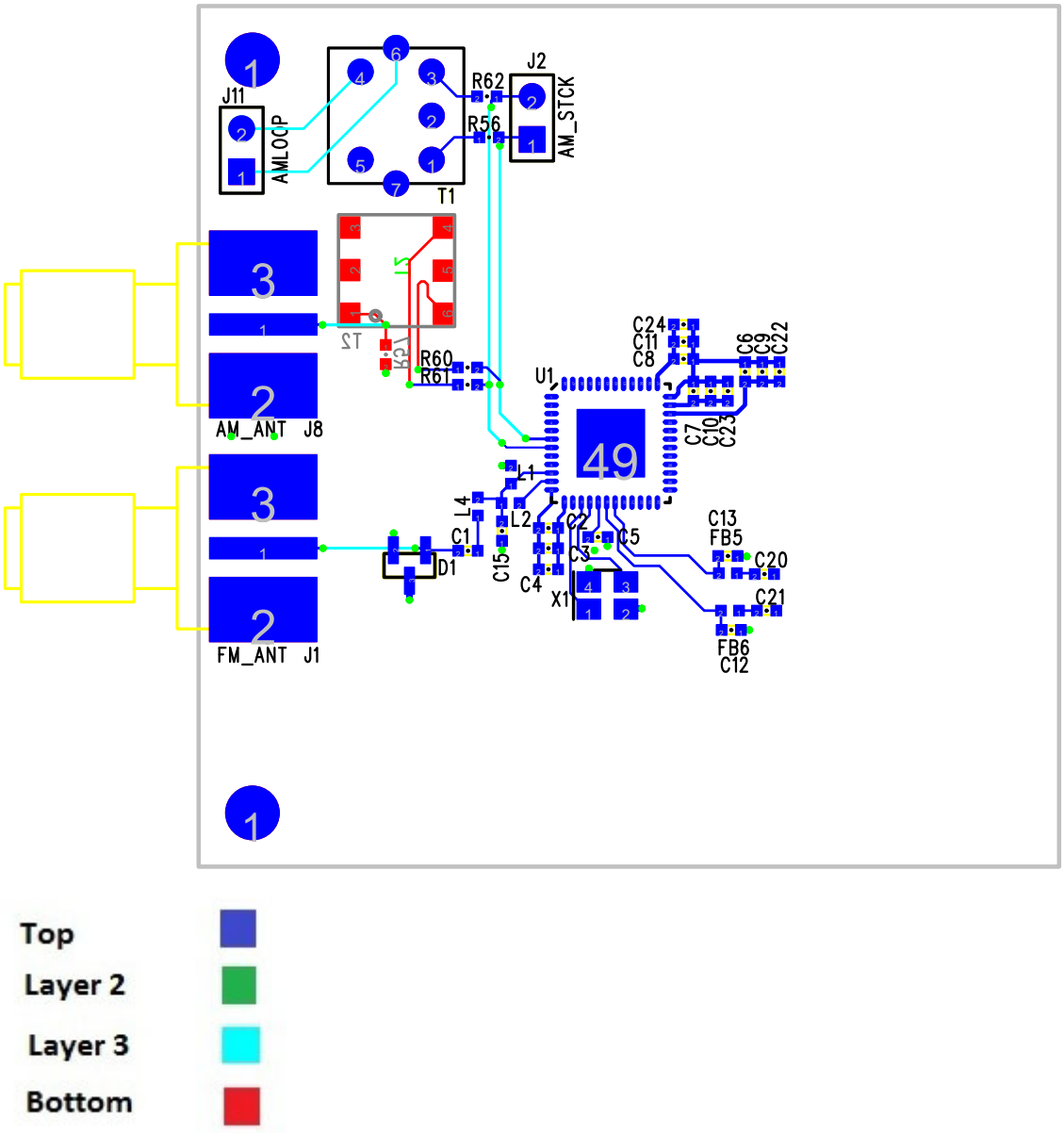


Figure 2. Si468x QFN Layout Design with Legend

Figure 2 shows Si468x layout with all 4 layers and crystal support. All bypass components are placed around the silicon as close as possible. A few things to note:

- The lowest value capacitor (8.2 pF) shall be placed the closest to the chip.
- Crystal and Audio traces shall be short in length and the recommended trace width is 6 mils.
- To minimize the loop area, all return currents shall be returned to its source as compactly as possible.

4. Antenna and Matching Network Design and Layout

4.1. HP Antenna (Si468x)

The Si468x Digital Radio Receiver component supports a headphone antenna interface through the VHFI pin. A headphone antenna with a length of 1.1 m suits FM/FMHD/T-DMB/DAB applications well.

4.1.1. Headphone Antenna Design

A typical headphone cable will contain three or more conductors. The left and right audio channels are driven by a headphone amplifier onto left and right audio conductors and the common audio conductor is used for the audio return path and RF antenna. Additional conductors may be used for microphone audio, switching, or other functions, and in some applications the RF antenna will be a separate conductor within the cable. A representation of a typical application is shown in Figure 3.

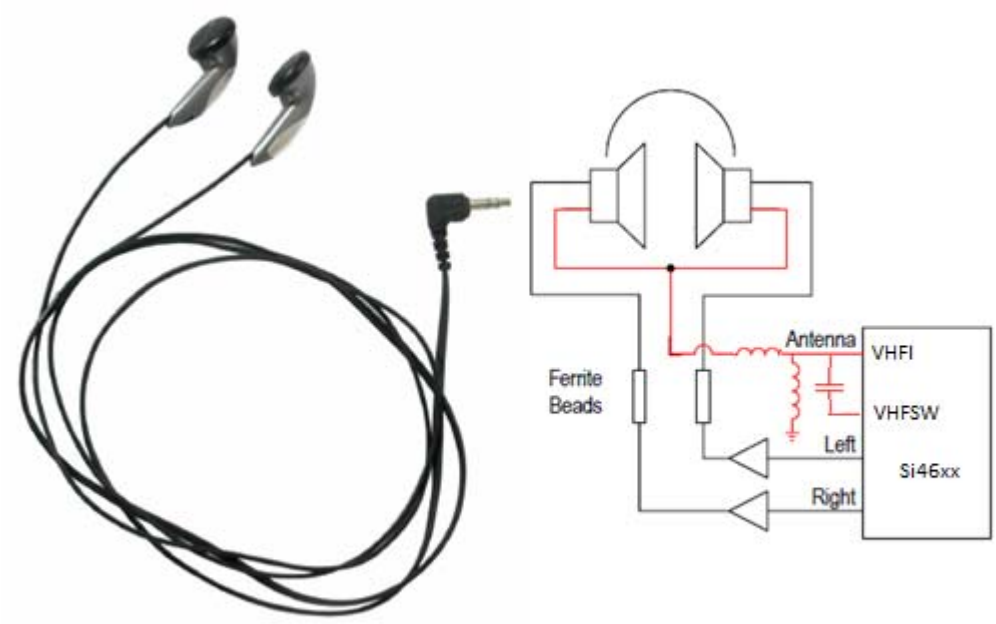


Figure 3. A Typical HP Antenna Application

4.1.2. Headphone Antenna Schematic

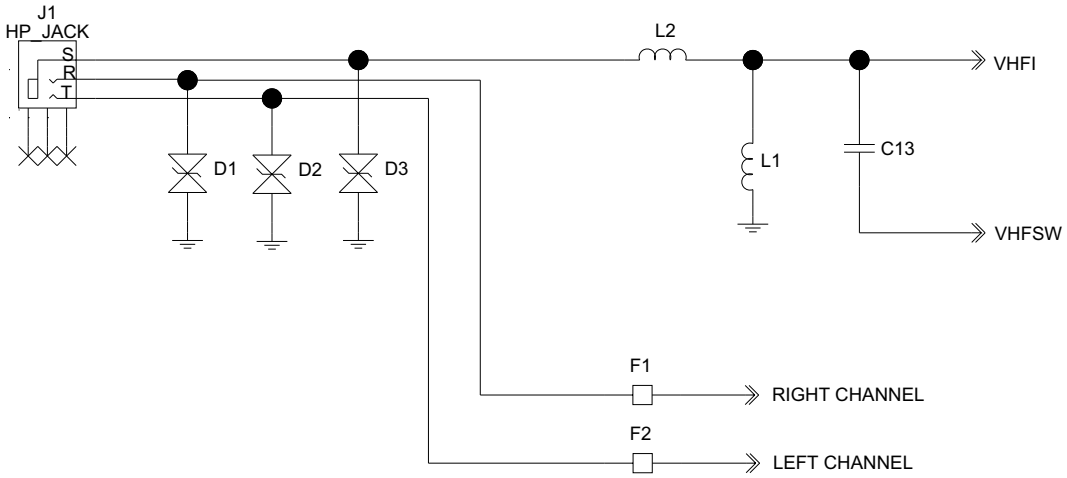


Figure 4. Headphone Antenna Design

The headphone antenna implementation requires components L1, L2, C13, F1, F2, and F3 for a minimal implementation. In Figure 4, a headphone and circuit with headphone audio common grounded is used. The ESD protection diodes and headphone amplifier components are system components that will be required for proper implementation of any tuner. Inductors 1 and 2 are selected to maximize the voltage gain across the DAB/T-DMB band. C13 is switched in with VFHSW to ensure the FM/FMHD band is properly resonated. The user should refer to property “0x1712” of AN649 to understand how to enable and disable the switch.

Ferrite beads F1 and F2 provide a low-impedance audio path and high-impedance RF path between the headphone amplifier and the headphone. Ferrite beads should be placed on each antenna conductor connected to nodes other than the VHFI such as left and right audio, microphone audio, switching, etc. In the example shown in the figure above, these nodes are the left and right audio conductors. Ferrite beads should be 2.5 kΩ or greater at 100 MHz, such as the Murata BLM18BD252SN1. High impedance is desirable to reduce antenna coupling to the other conductors.

L1 and L2 are used as audio ground. Diodes should be chosen with no more than 1 pF parasitic capacitance, and diode capacitance should be minimized. If D1 and D2 must be chosen with a capacitance greater than 1 pF, they should be placed between the ferrite beads and the headphone amplifier to minimize PCB parasitic capacitance. This placement will, however, reduce the effectiveness of the ESD protection devices. Diode D3 may not be relocated and must therefore have a capacitance less than 1 pF. Note that each diode package contains two devices to protect against positive and negative polarity ESD events.

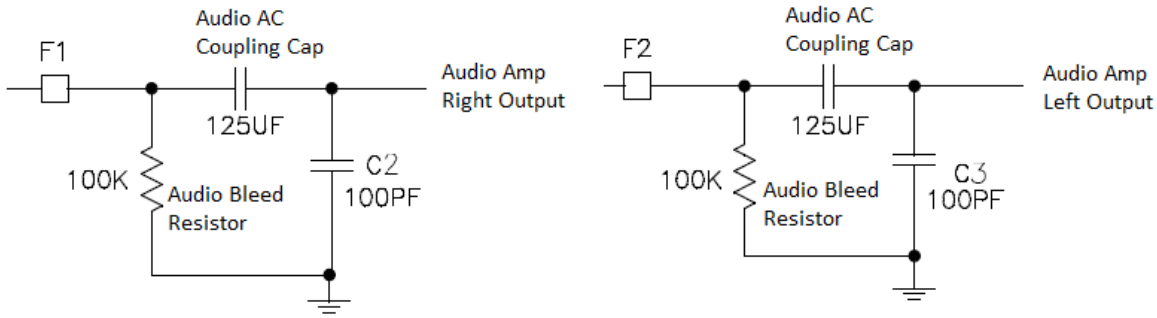


Figure 5. Optional RF Shunt Capacitors to Reduce Noise Coupling to Antenna

As shown in Figure 5, **optional** RF shunt capacitors C2 and C3 may be placed on the left and right audio traces at the headphone amplifier output to reduce the level of digital noise passed to the antenna. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

Table 2. Headphone Antenna BOM

Ref Designator	Description	Note
L1	IND, SM, 100 nH, MURATA	
L2	IND, SM, 36 nH, MURATA	
C13	AC coupling cap, SM, 18 pF, Murata	
F1, F2, F3	FERRITE BEAD, SM, 0603, 2.5 kΩ, Murata, BLM18BD252SNID	
D1, D2, D3	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213	

Table 3. Headphone Antenna Optional BOM

Ref Designator	Description	Note
C2	SM, 0402, X7R, 100 pF	Optional RF shunt capacitor
C3	SM, 0402, X7R, 100 pF	Optional RF shunt capacitor

4.1.3. Headphone Antenna Layout

To minimize inductive and capacitive coupling, inductors C13, L1 and L2 should be placed together close to the Si468x and as far from noise sources such as clocks and digital circuits as possible.

To minimize shunt capacitance on antenna trace, place ferrite beads F1 and F2 as close as possible to the headphone connector. To maximize ESD protection diode effectiveness, place diodes D1, D2, and D3 as close as possible to the headphone connector. If capacitance larger than 1 pF is required for D1 and D2, both components should be placed between F1, F2, and F3 and the headphone amplifier to minimize antenna shunt capacitance.

Place the chip as close as possible to the headphone connector to minimize antenna trace capacitance. Keep the trace length short and narrow and as far above the reference plane as possible, restrict the trace to a microstrip topology (trace routes on the top or bottom PCB layers only), minimize trace vias, and relieve ground fill on the trace layer. Note that minimizing capacitance has the effect of maximizing characteristic impedance. It is not necessary to design for 50 Ω transmission lines.

4.2. Cable antenna (Si468x)

The charger cable of a consumer product can be used as an FM/FMHD/T-DMB/DAB antenna. This section describes how to interface the Si468x VHFI input to a cable antenna.

4.2.1. Cable Antenna Design

A typical cable antenna contains multiple inner wires/conductors, which are covered with a protective ground shield. The coupling between the wires and the shield can cause the antenna to have large capacitance in the several hundred pF range. In order to boost the received FM/FMHD/T-DMB/DAB voltage, it is necessary to minimize this capacitance. This reduction can be achieved by placing ferrite beads in series with each of the antenna's conductors.

4.2.2. Cable Antenna Schematic

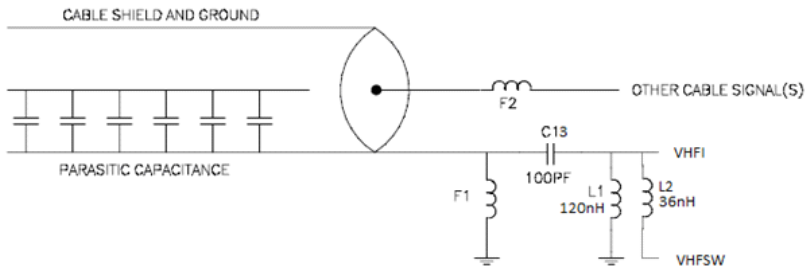


Figure 6. A Typical Cable Antenna Application

To resonate the cable antenna within the FM band, the antenna's capacitance needs to be reduced. As described in Section 4.2.1, this reduction can be achieved by placing the ferrite beads in series with each of the antenna's conductors. The capacitance should be further controlled by limiting the trace length from the cable ground shield and the RF input pin (VHFI input) on the Si468x digital radio chip. Each of the components in the schematic above is explained in detail below:

L1 (120 nH) is the tuning inductor. This is the typical value used to resonate the cable antenna in the center of the DAB Band.

L2 (36 nH) is the tuning inductor. This is the typical value used to parallel with L1 to resonate the cable antenna in the center of the DAB Band.

C13 (100 pF) is a dc blocking cap placed between the VHFI pin and the cable antenna ground.

F1(1.5 kΩ at 100 MHz) is a shunt ferrite to ground at the cable antenna side. A substantial amount of ground return current may flow through the cable antenna shield/ground because there are multiple conductors inside the cable along with power supply conductors. The ferrite will divert the ground return current of the cable antenna to go through the shunt ferrite rather than going through the tuning inductor and/or Si468x chip.

F2 (1.5 kΩ at 100 MHz) is a series ferrite placed on the signal conductor in the cable antenna. Note that series

ferrites should be placed on each signal conductor in the cable. The ferrite is used to isolate the signal conductors from the shield/ground. The choice of the ferrite is dependent upon the type of signal on each individual conductor. If the conductor is used to carry power, then a ferrite with a large dc current carrying capability should be used. Likewise, if the conductor is used to carry high frequency analog signals, make sure that the ferrite does not filter the high frequency.

Table 4. Cable Antenna BOM

Ref Designator	Description	Note
L1	IND, SM, 120 nH, MURATA	
L2	IND, SM, 36 nH, MURATA	
C13	AC coupling cap, SM, 0402, X7R, 100 pF	
F1	Shunt Ferrite bead, SM, 0603, 470Ω, 1 A, Murata, BLM18PG471SN1J	Rated dc current> max expected ground return current.
F2	Series Ferrite bead, various types. Recommended ferrite for power lines: FERRITEBEAD, SM, 0603, 470Ω, 1 A, Murata, BLM18PG471SN1J Recommended ferrite for signals: FERRITEBEAD, SM, 0603, 2.5kΩ, 50mA Murata, BLM18BD252DN1D	For power signals, make sure the rated dc current> max expected ground return current. For all other signals, make sure ferrite does not block/filter the high frequency component of the signals.

4.2.3. Cable Antenna Layout

Place the chip as close to the cable antenna as possible. This will minimize the trace length going to the cable antenna which will minimize the parasitic capacitance. Place the shunt ferrite for the ground return current as close to the cable as possible. Putting the shunt ferrite for the ground return current close to the cable ensures that the ground return current has minimal loop which will reduce noise coupling. The series ferrites should be put as close as possible to the cable. This will minimize the parasitic capacitance seen by the VHFI pin.

5. Ferrite Loop Antenna for AM Receive on AMI

There are two types of antenna that will work well for an AM receiver: a ferrite loop antenna or an air loop antenna. A ferrite loop antenna can be placed internally on the device or externally to the device with a wire connection. When the ferrite loop antenna is placed internally on the device, it is more susceptible to picking up any noise within the device. When the ferrite loop antenna is placed outside a device, e.g., at the end of an extension cable, it is less prone to device noise activity and may result in better AM reception.

5.1. Ferrite Loop Antenna Design

Figure 7 shows an example of ferrite loop antennas. The left figure is the standard size ferrite loop antenna. It is usually used in products with a lot of space, such as desktop radios. The right figure is the miniature size of the loop antenna. It is usually used in small products where space is at a premium, such as cell phones. If possible, use the standard size ferrite loop antenna as it has a better sensitivity than the miniature one.

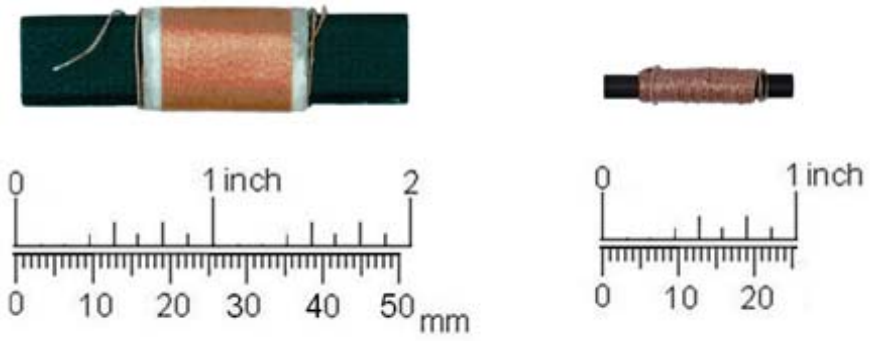


Figure 7. Standard and Miniature Ferrite Loop Antennas

A loop antenna with a ferrite inside should be designed such that the inductance of the ferrite loop is between 180 and 450 µH for the Si468x AM Receiver.

Table 5 lists the recommended ferrite loop antenna for the Si468x AM Receiver.

5.2. Ferrite Loop Antenna Schematic

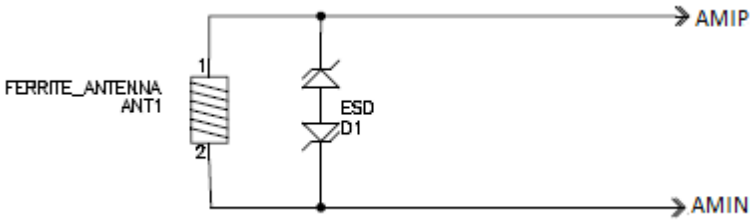


Figure 8. AM Ferrite Loop Antenna Schematic

D1 is an optional ESD diode if there is an exposed pad going to the AMI pin.

5.3. Ferrite Loop Antenna Bill of Materials

Table 5. Ferrite Loop Antenna Bill of Materials

Designator	Description	Note
ANT1	Ferrite loop antenna, 180–450 µH	
D1	ESD diode, IC, SM, SOT23-3, California Micro Devices, CM1213-01ST	Optional; only needed if the there is any exposed pad going to the AMI pin.

5.4. Ferrite Loop Antenna Layout

Place the chip as close as possible to the ferrite loop antenna feedline. This will minimize the trace going to the ferrite antenna which in turn will minimize parasitic capacitance, and also will minimize the possibility of noise sources coupling to the trace.

The placement of the AM antenna is critical, since AM is susceptible to noise sources causing interference in the AM band. Noise sources can come from clock signals, switching power supply, and digital activities (e.g., MCU). When the AM input is interfaced to a ferrite loop stick antenna, the placement of the ferrite loop stick antenna is critical to minimize inductive coupling. Place the ferrite loop stick antenna as far away from interference sources as possible. In particular, make sure the ferrite loop stick antenna is away from signals on the PCB and away from even the I/O signals of the Si468x. Do not route any signal under or near the ferrite loop stick. Route digital traces in between ground plane for best performance. If that is not possible, route digital traces on the opposite side of the chip. This will minimize capacitive coupling between the plane(s) and the antenna.

To tune correctly, the total capacitance seen at the AMI input needs to be minimized and kept under a certain value. The total acceptable capacitance depends on the inductance seen at the AM input. The acceptable capacitance at the AM input can be calculated using the formula shown in Equation 1.

$$C_{Total} = \frac{1}{(2\pi f_{max})^2 L_{effective}}$$

Equation 1. Expected Total Capacitance at AMI

Where:

C_{Total} = Total capacitance at the AMI input

$L_{effective}$ = Effective inductance at the AMI input

f_{max} = Highest frequency in AM band

The total allowable capacitance, when interfacing a ferrite loop stick antenna, is the effective capacitance resulting from the AMIP and AMIN input pins, the capacitance from the PCB, and the capacitance from the ferrite loop stick antenna. The inductance seen at the AMI pins in this case is primarily the inductance of the ferrite loop stick antenna. The total allowable capacitance in the case of an air loop antenna is the effective capacitance resulting from the AMI input pins, the capacitance of the PCB, the capacitance of the transformer, and the capacitance of the air loop antenna. The inductance in this case should also take all the elements of the circuit into account. The formula shown in Equation 1 gives a total capacitance of 29 pF when a 300 µH ferrite loop stick antenna is used for an AM band with 10 kHz spacing, where the highest frequency in the band is 1710 kHz.

5.5. Ferrite Loop Antenna Design Checklist

- ☐ **Place** the chip as close as possible to the ferrite loop antenna feedline to minimize parasitic capacitance and the possibility of noise coupling.
- ☐ **Place** the ferrite loop stick antenna away from any sources of interference and even away from the I/O signals of the Si468x. Please make sure that the AM antenna is as far away as possible from circuits that switch at a rate which falls in the AM band (520–1720 kHz).
- ☐ **Place** optional component D1 if the antenna is exposed.
- ☐ **Select** ESD diode D1 with minimum capacitance.
- ☐ **Do Not Place** any ground plane under the ferrite loop stick antenna if the ferrite loop stick antenna is mounted on the PCB. The recommended ground separation is 1/4 inch or the width of the ferrite.

6. Air Loop Antenna

An air loop antenna is an external AM antenna (because of its large size) typically found on home audio equipment. An air loop antenna is placed external to the product enclosure making it more immune to system noise sources. It also will have a better sensitivity compared to a ferrite loop antenna.

6.1. Air Loop Antenna Design

Figure 9 shows an example of an air loop antenna.

Figure 9. Air Loop Antenna

Unlike a ferrite loop, an air loop antenna will have a smaller equivalent inductance because of the absence of ferrite material. A typical inductance is on the order of 10 to 20 µH. Therefore, in order to interface with the air loop antenna properly, a transformer is required to raise the inductance into the 180 to 450 µH range.

T1 is the transformer to raise the inductance to within 180 to 450 µH range. A simple formula to use is as follows:

$$L_{equivalent} = N^2 L_{AIRLOOP}$$

Typically a transformer with a turn ratio of 1:5 to 1:7 is good for an air loop antenna of 10–20 µH to bring the inductance within the 180 to 450 uH range.

Choose a high-Q transformer with a coupling coefficient as close to 1 as possible and use a multiple strands Litz wire for the transformer winding to reduce the skin effect. All of this will ensure that the transformer will be a low loss transformer.

Finally consider using a shielded enclosure to house the transformer or using a toroidal shape core to prevent noise pickup from interfering sources.

A few recommended transformers are listed in Table 6.

Table 6. Recommended Transformers

	Transformer 1	Transformer 2	Transformer 3
Vendor	Jiaxin Dianzi	UMEC	UMEC
Part Number	SL9x5x4MWTF1	TG-UTB01527S	TG-UTB01526
Type	Surface Mount	Surface Mount	Through Hole
Primary Coil Turns (L1)	12T	10T	10T
Secondary Coil Turns (L2)	70T	55T	58T
Wire Gauge	ULSA / 0.07mm x 3	n/a	n/a
Inductance (L2)	380 µH ±10% @ 796 kHz	184 µH min, 245 µH typ @ 100 kHz	179 µH min, 263 µH typ @ 100 kHz
Q	130	50	75

The following is the vendor information for the above transformer:

Vendor #1:

Jiaxin Dianzi

Guangzhou Jiaxin Electronics Shenzhen Sales Office

email: sales@firstantenna.com

Web: www.firstantenna.com

Vendor #2:

UMEC USA, Inc.

Website: www.umec-usa.com

www.umec.com.tw

6.2. Air Loop Antenna Schematic

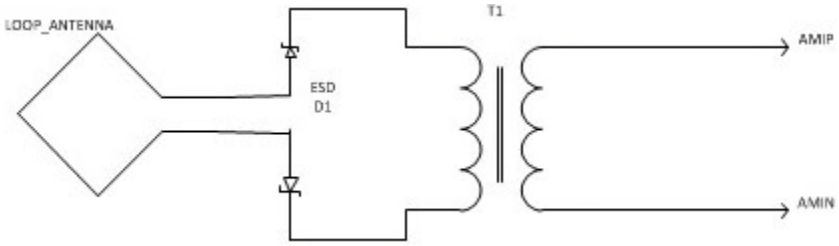


Figure 10. AM Air Loop Antenna Schematic

D1 is a required ESD diode since the antenna is exposed.

6.3. Air Loop Antenna Bill of Materials

Table 7. Air Loop Antenna Bill of Materials

Designator	Description	Note
LOOP_ANTENNA	Air loop antenna	
T1	Transformer, 1:6 turns ratio	
D1	ESD diode, IC, SM, SOT23-3, California Micro Devices, CM1213-01ST	

6.4. Air Loop Antenna Layout

Place the chip and the transformer as close as possible to the air loop antenna feedline. This will minimize the trace going to the air loop antenna which in turn will minimize parasitic capacitance and the possibility of noise coupling.

When an air loop antenna with a transformer is used with the Si468x, minimize inductive coupling by making sure that the transformer is placed away from all sources of interference. Keep the transformer away from signals on the PCB and away from even the I/O signals of the Si468x. Do not route any signals under or near the transformer. Use a shielded transformer if possible.

6.5. Air Loop Antenna Design Checklist

- ☐ **Select** a shielded transformer or a toroidal shape transformer to prevent noise pickup from interfering sources
- ☐ **Select** a high-Q transformer with coupling coefficient as close to 1 as possible
- ☐ **Use** multiple strands Litz wire for the transformer winding
- ☐ **Place** the transformer away from any sources of interference and even away from the I/O signals of the Si468x. Please make sure that the AM antenna is as far away as possible from circuits that switch at a rate which falls in the AM band (520–1720 kHz).
- ☐ **Select** ESD diode D1 with minimum capacitance.

APPENDIX A—PROCEDURE TO OPTIMIZE CONDUCTED SENSITIVITY THROUGH VARACTOR TUNING

There are 3 properties related with varactor-tuning procedure in each image:

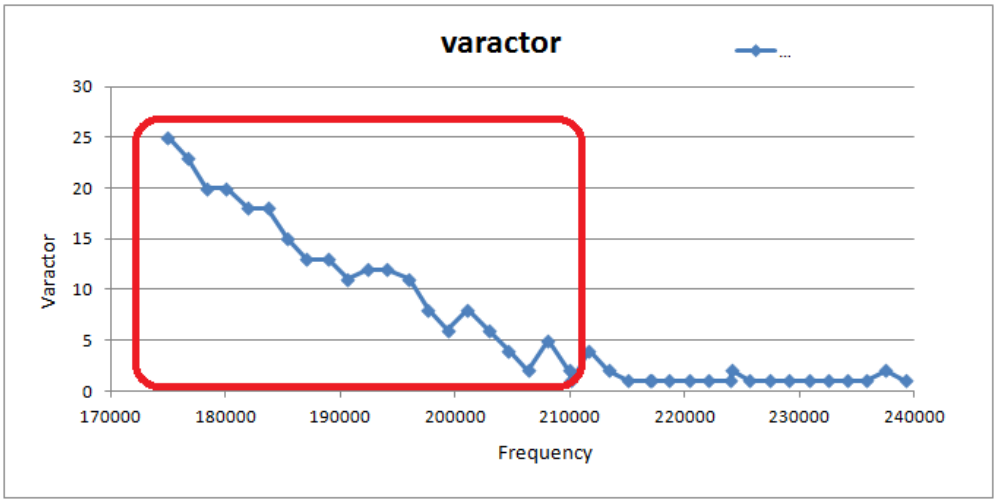
Table 8. Varactor Tuning Properties

ID	FM/DAB	Note*
0x1710	FM/DAB_TUNE_FE_-VARM	Slope of Varactor vs Frequency Curve
0x1711	FM/DAB_TUNE_FE_-VARB	Intercept of Varactor vs Frequency Curve
0x1712	FM/ DAB_TUNE_FE_CFG	Configure VHFSW switch from open to close
***Note:** See AN649 for detailed descriptions of these properties.		

The following procedure is intended to show how to achieve the best conducted sensitivity result for Si468x for FM/DAB band by tuning the on-chip varactor. The end goal is for the customer to identify the desired values of the above 3 properties in each functional FW image. After the part is booted, the 3 properties are set to 0 by default. For each PCB design, the customer needs to set identified values so that the customer can use the automatic tuning function to achieve the target of conducted sensitivity specification.

In the tuning command of FM/DAB image (FM/DAB_TUNE_FREQ), there is an ANTCAP parameter. Once the ANTCAP is issued with the tuning command as any value other than 0, the automatic tuning function (determined by VARM/VARB settings) is bypassed and the on-chip varactor is set as the ANTCAP value as specified by users. This feature is utilized in the procedure described below for DAB.

- Set DAB_TUNE_FE_CFG property as 1, which closes the VHFSW.
- How to optimize varactor value for each individual frequency X:
  1. Connect the signal-generator to DUT with an SMA barrel.
  2. Set the signal-generator to frequency X with 40 dBuV rf level and FM/DAB modulation.
  3. Tune Si468x to frequency X with ANTCAP set to 1.
  4. Call Test_Get_RSSI command 5 times and get the average of the 5 RSSi measurements.
  5. Increment the ANTCAP by 1 and re-issue the tune command to Si468x.
  6. Repeat Step 4 and Step 5 until reaching the max tunable varactor range of 128.
  7. Identify the varactor value with the max RSSI reading.
- Repeat the test for frequencies across the DAB band.
- If describing the varactor's relationship with frequency by varactor_value=m/1000*frequency (in MHz) +b, m represents the slope (DAB_TUNE_FE_VARM), b represents the intercept (DAB_TUNE_FE_VARB). Given the data collected, identify the low frequency range where the optimal varactor is not lower than 4. This is illustrated in the graph* below.



***Note:** This graph is taken with Silicon Laboratories' Si468x WLCSP daughtercard, version 2.0

Figure 11. Varactor vs. Frequency Chart

- Feed this data section in red circle to linear-fit algorithm to identify the slope m and intercept b. Program m and b values into the properties: 0x1710, 0x1711 after Si468x is booted.
- When tuning, issue the "dab_tune_freq 0 $freq 0" to enable automatic tuning method.

APPENDIX B—GUIDE TO TUNE THE FRONT END NETWORK

Analyzing the Front End

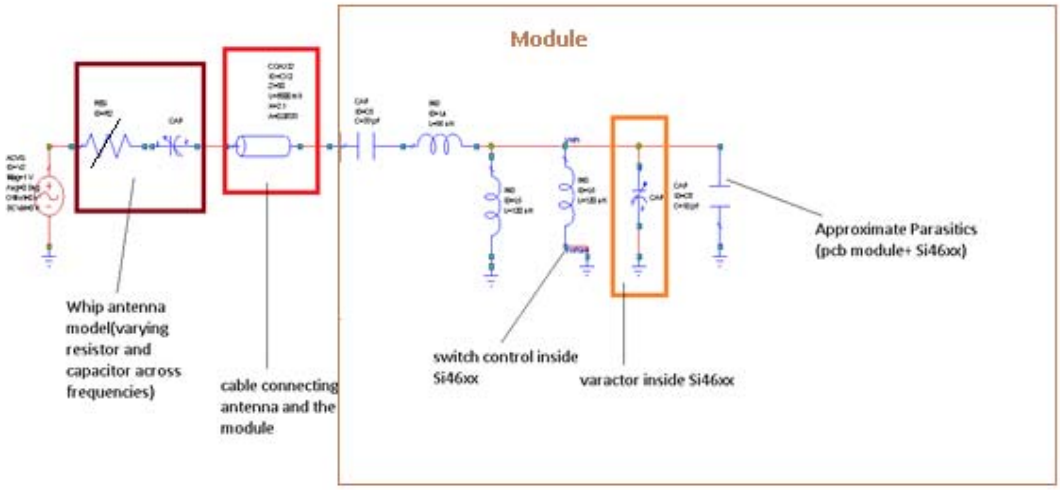


Figure 12. Antenna Interface with Module FE

Figure 12 shows the electrical model of telescopic antenna connected to the front end of the module via coax cable. The telescopic antenna is electrically represented by a variable resistor and a variable capacitor. The electrical representation of coax cable is capacitor to ground. The length of the cable becomes important to consider when selecting the front end component values. The interface of antenna and cable with module front end can be simplified into Norton equivalent as shown in Figure 14.

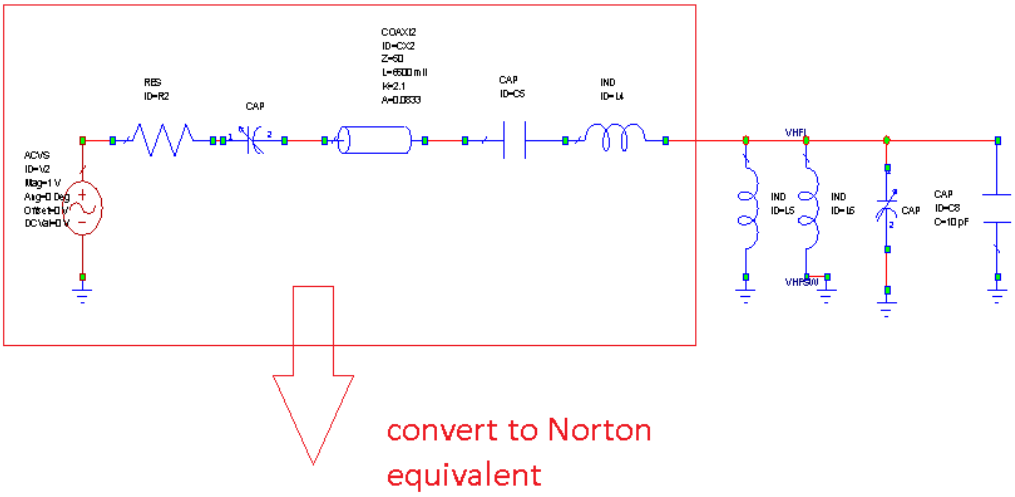


Figure 13. Antenna Interface with Module FE

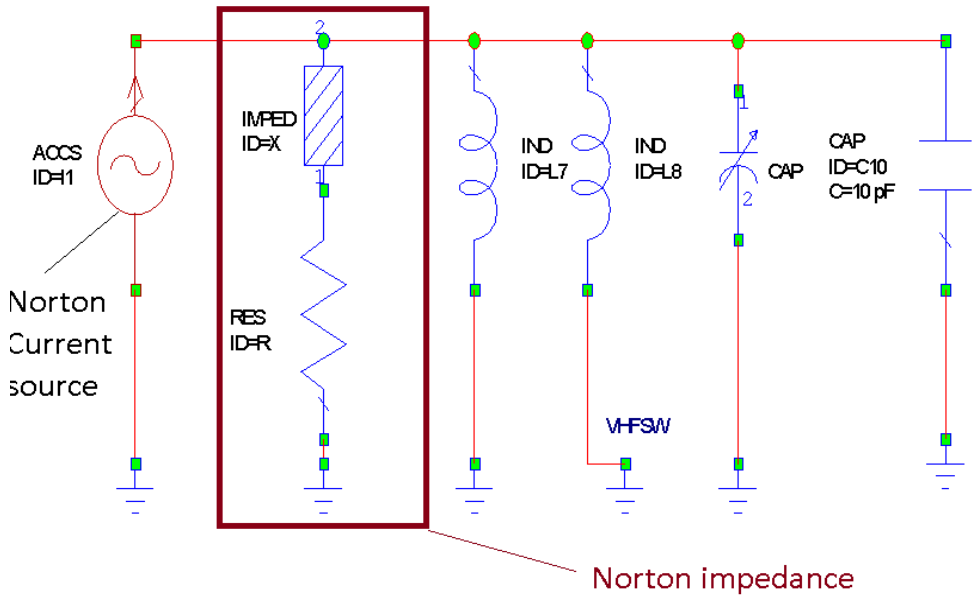


Figure 14. Norton Equivalent of Antenna Interface with Module FE

The reactance part of the Norton impedance branch can be capacitive or inductive. The complex impedance of the Norton branch depends on the following things:

(a) The front end series LC circuit (Ref designator C5 and L4)

(b) Type of antenna and ground plane, if any

(c) Length of the cable
(d) Band (FM/DAB)
(e) Frequencies within the band

The Figure 14 network can be further simplified into the simple parallel RLC circuit shown in Figure 15. The transformation (series to parallel at single frequency) helps convert the Norton branch into its parallel equivalent shown below. The network shown in Figure 15 is a simplified representation of parallel LC tank circuit with inductors and capacitors in parallel. For a given frequency, using resonance frequency equation $F=1/2\Pi\sqrt{LC}$, an unknown quantity (inductor or capacitor) can be calculated.

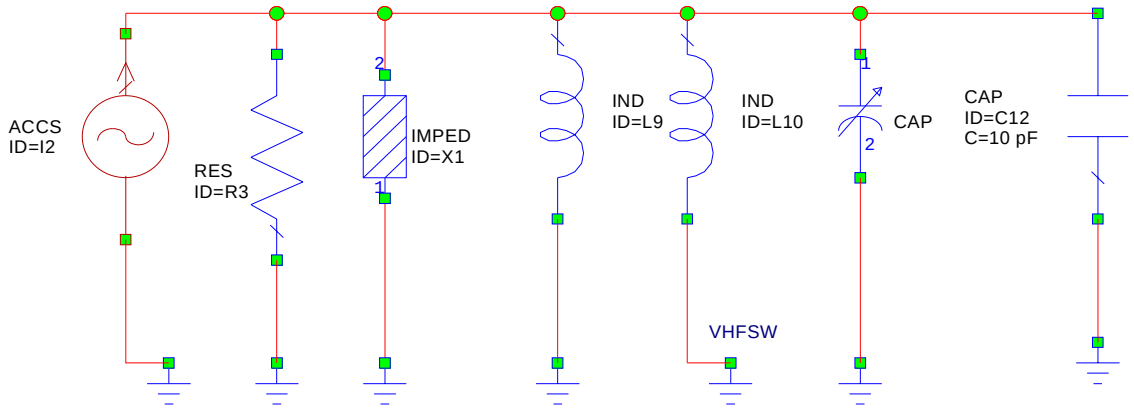


Figure 15. Parallel RLC

Optimization of Front End

Silicon Labs recommends using its EVB and the GUI to optimize the front end for a given antenna type and the cable length. The GUI has an antenna graph function, shown in Figure 16, which exercises the internal varactor capacitor across its range (1–128 counts) for finding the capacitance required to form resonance at a given frequency.

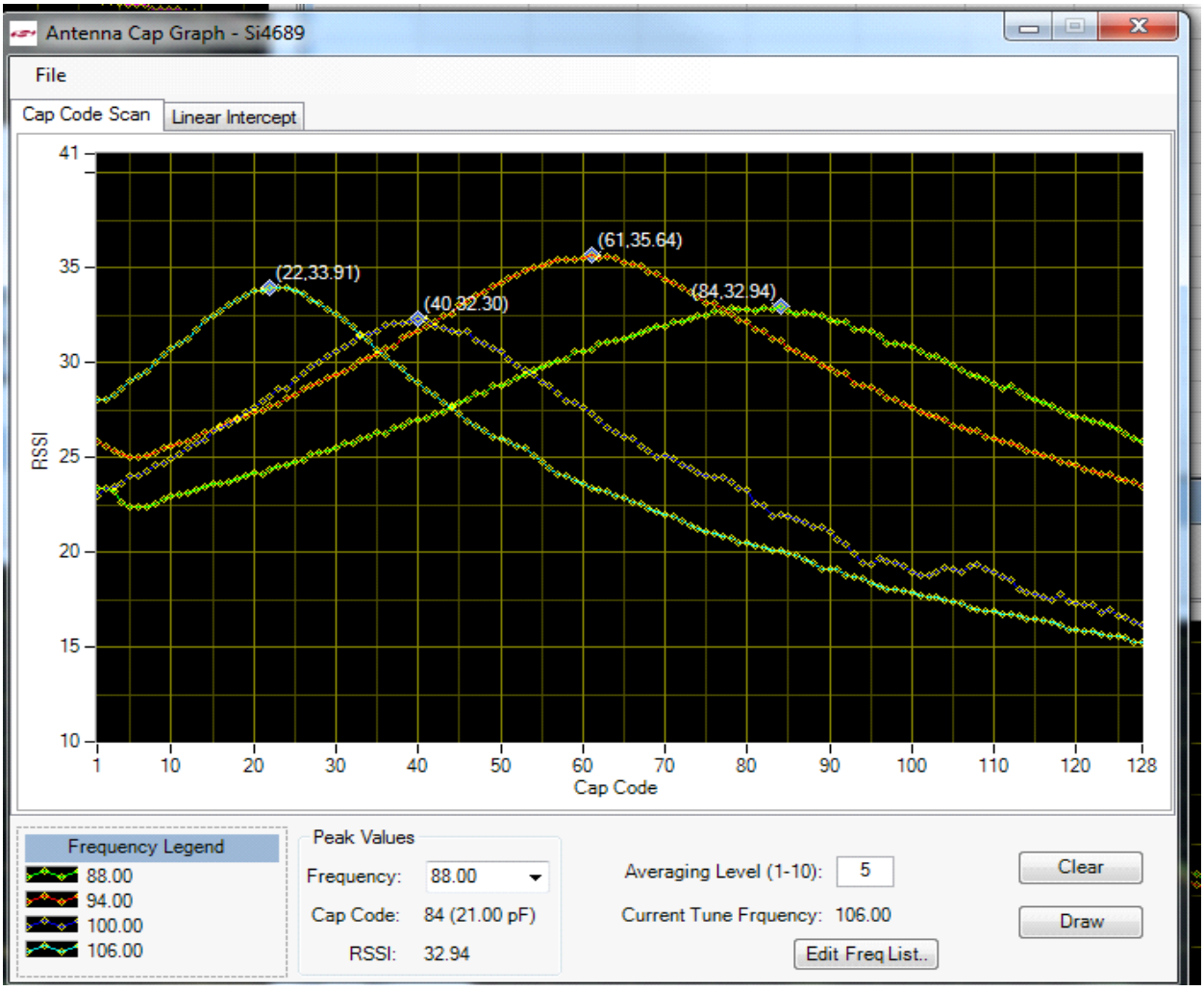


Figure 16. GUI Antenna Cap Graph for FM

The process stated below should be applied to three frequencies (Low, Mid and High) within a given band.

1. Initially use the Silicon Labs-recommended values for C1 (33pf) and L1 (56nh) shown in Figure 16.

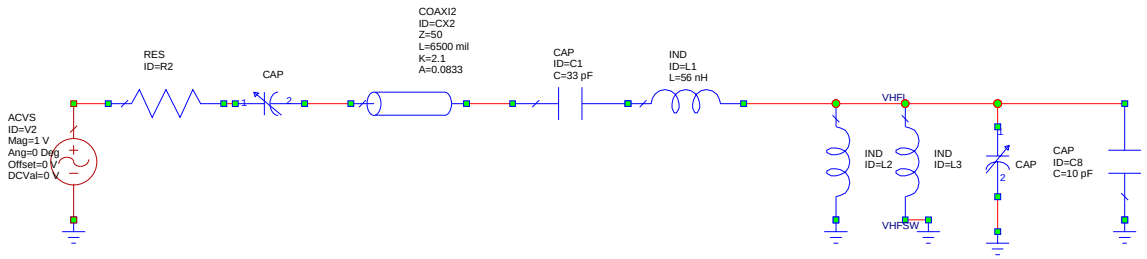


Figure 17. Antenna Interface with Module FE

2. Measure the impedance of the antenna using network analyzer (S11 measurement). Write down the resistive and reactance values.
3. Measure the impedance of the cable.
4. Convert the above circuit into a simplified parallel LC circuit (shown in previous section).
5. Choose and fix the shunt indicator (L2 value) and then calculate the capacitance required using resonance frequency equation $F=1/2\Pi\sqrt{LC}$ at the lowest frequency.
6. Use the antenna graph function of Si46xx EVB GUI to measure the capacitance value required to form resonance by engaging internal varactor.
   a. Verify the capacitance calculated in step 5 (circuit analysis) approximately equals the capacitance calculated by GUI minus the parasitic capacitance (PCB + Si46xx front end).
7. Ideally, to form resonance across the entire band, the varactor capacitance required at low frequency should be close to its maximum value 32pf (128 varactor counts).
8. Change L2 if the varactor capacitor measured at low frequency is not close to its max value of 32pf (128 counts). The inductor L2 may not have any impact in forming resonance at low frequency within the band because the inductive reactance in the Norton branch (shown in the previous section) may be dominating.
9. Change C1 or L1 and repeat steps 4 through 8.
10. Verify that with chosen values of C1, L1, and L2 the entire range of varactor capacitor is put in use across the frequency band.
11. For tuning across a different band, the inductor switch VHFSW option shall be exercised to engage L3 inductor keeping other component values fixed. For forming resonance within this band, choose a value for L3 and follow steps 2 through 9.

The single optimized network for multiple band (FM and DAB) usage shall be formed after repeating the above process two to three times.

Silicon Labs Recommended Front End Network

Silicon Labs recommends using the front end network shown in Figure 18. The component values (C1-33pf, L1-56nh, L2-120nh, and L3-120nh) are optimized to use with fully extended telescopic antenna (24 inches) and 6.5 to 7-inch length of coax cable connecting the antenna and the module.

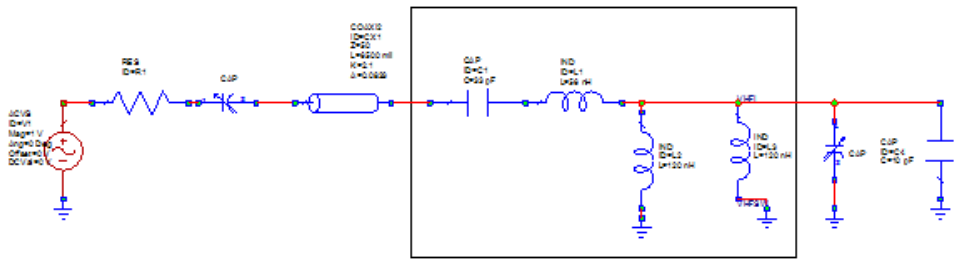
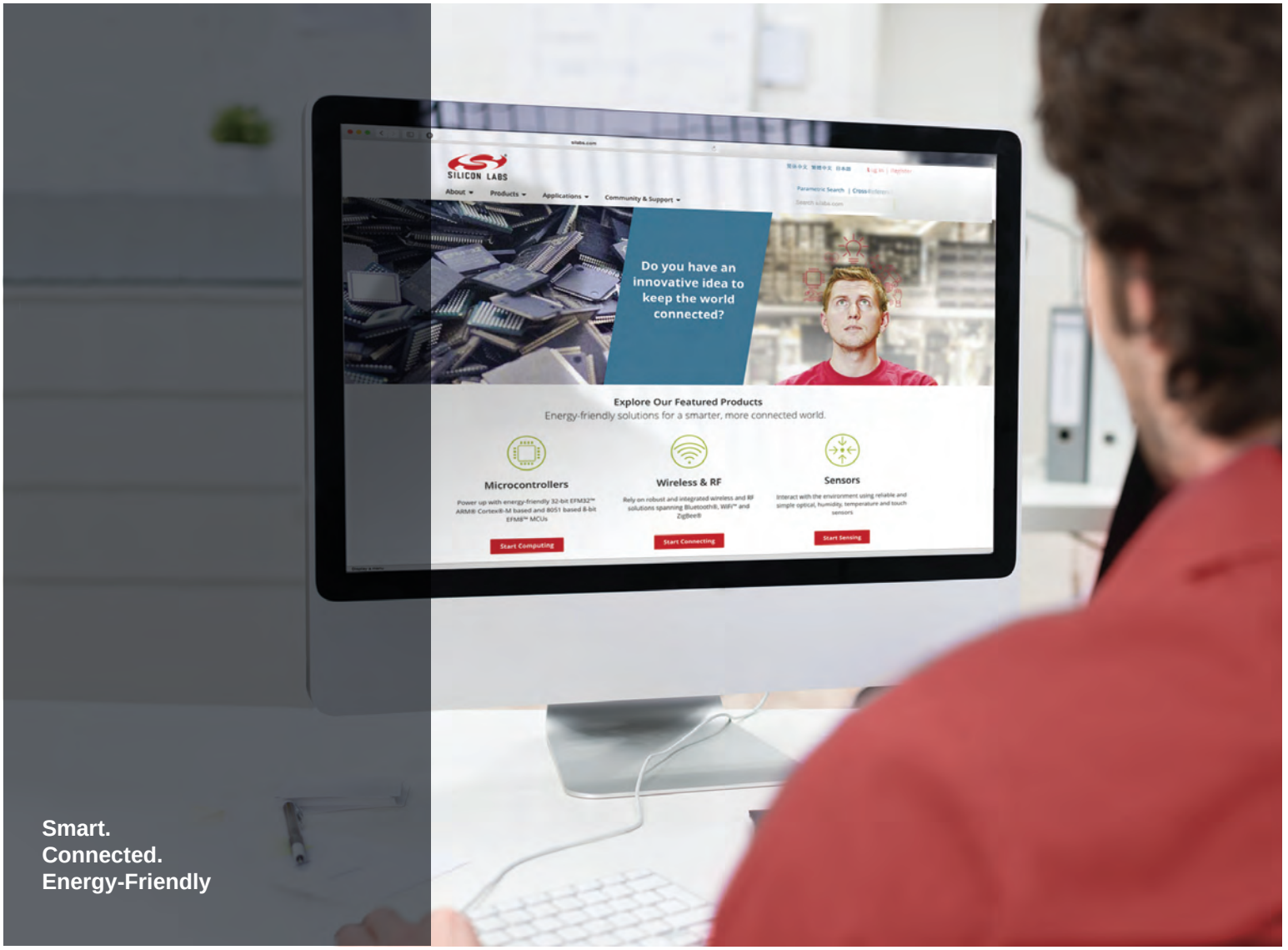


Figure 18. Silicon Labs Recommended FE Network

The varactor capacitor slope and intercept, and VHFSW switch API properties for the recommended network shall be set to the following:

FW Image	Slope (property 0x1710)	Intercept (property 0x1711)	Switch(property 0x172)
FM	0xEDB5	0x01E3	1 (closed)
DAB	0xF8A9	0x01C6	1 (closed)

If the VHFSW switch position required for both FM and DAB band is the same (close—as in the above network) then L2 and L3 can be replaced with a single inductor equivalent to the parallel combination of L2 and L3.



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