Errata Note

SX1276/77/78 – 137 to 1020 MHz
Low Power Long Range Transceiver

Revision 1 - Sept 2013

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1 Chip Identification - Disclaimer

SX1276, SX1277 and SX1278 are Production Released, with silicon Version 1b, identified as follows:

RegVersion at address 0x42 returns value 0x12

This note describes the behavior of silicon version V1b only.

Should you have any questions regarding the content of this document, or any other questions, please contact your Semtech sales representative.

Note:
The devices of previous silicon revision V1a are engineering samples which do not offer full functionality. They should not be used in a production device.

2 LoRa Modem

2.1 Sensitivity Optimization with a 500 kHz Bandwidth

Description
Some of the default settings of the LoRa modem should be manually modified to optimize the sensitivity of the product when the bandwidth is set to 500 kHz.

Workaround
The following LoRa registers should be changed as described, for BW=500 kHz

- For carrier frequencies ranging from 862 to 1020 MHz
  - Set LoRa register at address 0x36 to value 0x02 (by default 0x03)
  - Set LoRa register at address 0x3a to value 0x64 (by default 0x65)

- For carrier frequencies ranging from 410 to 525 MHz
  - Set LoRa register at address 0x36 to value 0x02 (by default 0x03)
  - Set LoRa register at address 0x3a to value 0x7F (by default 0x65)

For all other combinations of bandwidth / frequencies, register at address 0x36 should be re-set to value 0x03, and the value at address 0x3a will be automatically selected by the chip.

2.2 Frequency Offset Tolerance with 500 kHz Bandwidth

Description
With LoRa bandwidth set to 500 kHz, and with the largest spreading factors (SF=10,11,12), the tolerance to frequency offset is limited to +/-60 kHz

Workaround
No workaround identified.

2.3 Receiver Spurious Reception of a LoRa Signal

Description

The SX1276/77/78 receiver may receive other LoRa signals at a defined frequency and level. For it to happen, the interfering LoRa signal must have the same bandwidth and spreading characteristics as the actual modem settings.

Workaround

The phenomenon can be mitigated by changing the Intermediate Frequency of the receiver, as per Table 1:

Table 1: Settings for Optimized Receiver Response

	LoRa BW Setting									
	7.81kHz	10.42kHz	15.62kHz	20.83kHz	31.25kHz	41.67kHz	62.5kHz	125kHz	250kHz	500kHz
Bit 7 at address 0x31 (default = 1)	0	0	0	0	0	0	0	0	0	1
Value at address 0x2F	0x48	0x44	0x44	0x44	0x44	0x44	0x40	0x40	0x40	-
Value at address 0x30	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	-
Offset Frf(23:0) by	+7.81kHz	+10.42kHz	+15.62kHz	+20.83kHz	+31.25kHz	+41.67kHz	-	-	-	-

As shown, the Local Oscillator frequency as well as other registers related to the IF setting of the device have to be modified. Proceed as follows:

1) Set the device to Sleep or Stdby mode
2) Offset Frf as appropriate
3) Set bit 7 at address 0x31 to the correct value
4) Set new values at addresses 0x2F and 0x30
5) The device is now all set for improved rejection

Note that these bits will be reset at POR or after a Manual Reset sequence. Also, it is required to reprogram values at addresses 0x2F and 0x30 in the event that bit 7 at address 0x31 is re-set to 1 (this would automatically erase any previous value set in those registers).

The following improvement will result:

Table 2: Optimized Rx Spurious Response

	LoRa BW Setting									
	7.81kHz	10.42kHz	15.62kHz	20.83kHz	31.25kHz	41.67kHz	62.5kHz	125kHz	250kHz	500kHz
Offset of Spurious Reponse	+/-62.5kHz	+/-83kHz	+/-125kHz	+/-167kHz	+/-250kHz	+/-333kHz	+/-500kHz	+/-1MHz	+/-2MHz	
Worst case (SF=12) estimated level causing spurious reception (LoRa signal with same BW/SF)	>-90dBm*	>-70dBm*	>-60dBm*	>-65dBm*	>-80dBm	>-75dBm	>-15dBm	>-15dBm	>-15dBm	No response
* SF9 or less, reasonable data rate at the lowest BW										

Note: these numbers represent worst case situations, which correspond to the lowest SX1276/77/78 sensitivities. Those are observed with Spreading Factor set to 12. With SF = 7, the response will be approximately 15dB higher than tabulated.

2.4 Valid Packet Counter Offset

Description
The valid packet counter (used for debug, and counting only packets whose CRC is correct) presents the following issue:

- In Rx Single mode, it does not increment
- In Rx Continuous mode, it does not count the first valid packet received

Workaround

- In Rx Single mode, do not use this counter, but instead increment a counter variable if *PayloadCrcError=0* on a *RxDone* interrupt.
- In Rx Continuous mode, the same method can apply.

3 FSK Modem

3.1 PayloadReady Set for 31.25ns if FIFO is Empty

Description
When receiving in Packet mode with the SX1276/77/78, the microcontroller can be instructed to service the FIFO and read the bytes it contains before the *PayloadReady* flag is set, thanks to the *FifoLevel* gauge. On the SX1276/77/78, the duration of *PayloadReady* is very short (31.25ns) if the FIFO is already emptied at packet end, when this interrupt fires.

This situation can happen if *FifoThreshold* and the corresponding *FifoLevel* interrupts are used to monitor the FIFO content and offload it on-the-go, *FifoThreshold* being equal to the number of bytes stored in the FIFO.

Workaround
When *FifoLevel* interrupt is used to offload the FIFO, the microcontroller should monitor both PayloadReady and *FifoLevel* interrupts, and read only (*FifoThrehold*-1) bytes off the FIFO when *FifoLevel* fires.

3.2 Erroneous IBM Data Whitening/De-Whitening

Description
On the SX1276/77/78, the implementation of the IBM-compatible whitening/de-whitening algorithm is erroneous, which makes it incompatible with the standard implementation.

Conditions:

- ✓ *CrcWhiteningType* = 1
- ✓ *DcFree* = 10

Workaround
The workaround is to use “unlimited Length Packet Format”, and process whitening/de-whitening in the host microcontroller. Semtech is providing software implementations of this algorithm. Please contact your Semtech representative for assistance.

4 Revision History

Revision	Date	Silicon Revision	Description/Changes
1	Sept 2013	V1b	Final release

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