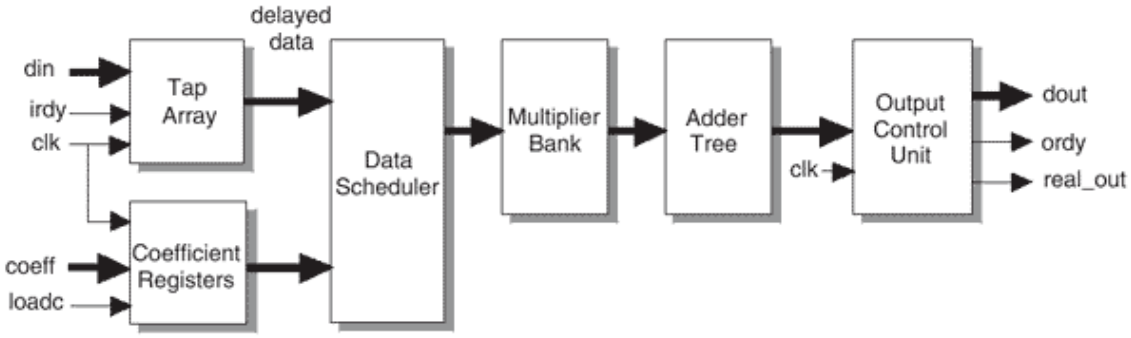
Parallel FIR Filter

Overview

Many digital systems use filters to remove noise, provide spectral shaping, or perform signal detection. Two common filters that provide these functions are Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. IIR filters are used in systems that can tolerate phase distortion. FIR filters are used in systems that require linear phase and have an inherently stable structure. For this reason, FIR filters are designed into a large number of systems.

The Parallel FIR Filter core can perform filtering with zero latency and is well suited for real-time applications. The core supports two modes of computation/filtering: single-cycle and multi-cycle. In single-cycle, filtering is done in one clock cycle and in multi-cycle, filtering is accomplished in multiple clock cycles.



Features

- Variable number of taps up to 64
- Data and coefficients up to 32 bits
- Output size consistent with data size
- Zero-latency operation
- Signed or unsigned data and coefficients
- Full Arithmetic Precision
- Fixed or loadable coefficients
- Decimation and interpolation
- Real or complex data
- Selectable rounding
- Scaleable outputs
- Fully parallel implementation
- Multi-cycle modes for area/time tradeoffs
- Optimization based on symmetry of filter
- IP core package
  - Data sheet and user's guide
  - Functional simulation models
  - Lattice netlist

Evaluation Configurations

Performance and Resource Utilization[1]

Parameter File	Parameter	LUT4s[2]	ispXPGA PFUs[3]	Registers	External Pins	System EBRs	f_{MAX}[1] (MHz)
fir_para_xp_1_002.lpc	See Below	858	297	149	31	None	51

[1] Performance and utilization characteristics are generated using LFX1200B-04FE680C in Lattice's ispLEVER™ v.3.0 software. Synthesized using Synplicity's Synplify Pro v.7.1. When using this IP core in a different density, package, speed, or grade within the ispXPGA family, performance may vary slightly.

[2] Look-Up Table (LUT) is the standard logic block of the ispXPGA. LUT4 is a 4-input LUT.

[3] Programmable Function Unit (PFU) contains LUTs and other resources.

Description of Netlist Configuration

Parameter File Name	Input Data Width	No. of Taps	FIR Type	Symmetry	Arithmetic Type	Data Type	Output Data Width (Full data width)	Fixed Coefficients
fir_para_xp_1_002.lpc	8 bits	16	Single cycle	Symmetric	Signed	Real	Full (21)	60, 44, D9, 37, 35, 16, F6, 39 (HEX)

Ordering Information

Part Numbers: For ispXPGA: FIR-PARA-XP-N1

To find out how to purchase the 32 Bit PCI Target IP Core, please contact your **local Lattice Sales Office**.